TARGET

M. SYM ALL

- mechanic:
  - design nearly completed (forks)
  - parts are ordered
  - test setup prepared in Dortmund
  - ready beginning of 2001
  - installation april 2001
- counters:
  - design of new counters nearly finished
  - parts to be ordered within next weeks
  - test setup under installation in Dortmund (new diploma student)
  - old counters will be checked
- electronic:
  - revision ongoing
  - cooling enhanced
- software:
  - DAQ
  - analysis
  - database
  - steering

Bernhard Schwingenheuer Technical Board 9 Nov 2000

VDS Report

Reminder:

- 2 planes in SL8 dead
- 2 planes in SL1 dead (pot 103)
- few percent of Helix chips dead
- detector modules at about 12 mrad
- Aluminum caps for SL7 thick

Plans:

- keep almost all modules for 2001 (no sizable rad damage)
- repair SL8 modules if possible
- replace Helix2.1 with Helix3.1 (no wake up problem)
  start with pot 103 = SL1-3 of -x quadrant
- replace RF shield: 12.7 mm wide stainless steel bands by 7 mm wide bands of the same thickness, no more mechanical constraints for 10 mrad detector positioning
- develop new production procedure for thin SL7 Al caps

Status:

- no real progress on caps
- 7 mm stainless steel bands delivered, Al coating to improve conductivity in preparation
- Helix3.1 available, first hybrids are fabricated, timing not yet understood
- important progress on internal VDS alignment by Martin, regenerate constants for all runs

Technical Board Meeting
November 9, 2000
DESY Hamburg

OTR Repair Status

H. Kapitza

Topics:

1. OTR Repair Status
2. OTR Repair Statistics
3. OTR Tests

OTR Repair Status

Step	TC2+	TC1+	PC4+	PC3+	PC2+	PC1+	TC2–	TC1–
disassembly	✔	✔	✔	busy	✔	✔	Dec	✔
C exchange	Apr	✔	✔	Nov	busy	✔		✔
build mod.		1	3			3		4
repair/test		✔	busy		Nov	✔		✔
reassembly		busy	Nov			✔		✔
operation		Nov				busy		busy

- All PC– and TC2– will be disassembled during the service week (Dec 2–10).
- TC2– will undergo reduced testing program.
- All MC will be disassembled not before 2001.

OTR Repair Statistics

- **HV fault statistics:**

fault	PC1+	TC1−	TC1+
C_{comm}	26	22	29
C_1	13		7
short	2		6
other	8		10
total	49	53	52

- **Cut wire statistics:**

test	PC1+	TC1−	TC2−
old	20	60	61
new	17	65	71
total	37	125	132

OTR Tests

1. Comparative study old vs. new chambers:

chamber(s)	PC2/3±	PC1+
HV	1700/1900 V	
time [h]	476	346
short	5	1
unstable	1	1
total	6	2

2. Running at elevated voltages: 15 % gain increase for 1 % HV increase:

HV			
%	5 mm	10mm	Gain
100	1700	1900	32 000
102	1735	1940	42 000
104	1770	1975	56 000
106	1800	2015	74 000
108	1835	2050	98 000
110	1870	2090	130 000

Measurement schedule:

Date		PC1+	PC2+	PC3+	PC2−	PC3−
Sat	04	104	104	104	100	100
Sun	05	106	106	106	100	100
Mon	06	108	-	108	-	100
Tue	07	110	-	110	-	100
Wed	08	110	-	110	-	100
Thu	09	110	-	-	-	-
...	..	110	continue with PC1+ only			

$\rightsquigarrow$ 1 instability in PC1+

$\rightsquigarrow$ **1 short** in PC2+

High-Pt (outer chambers) Status

Noise Study :

- Threshold Shift

  ⇨ Not Significant as suspected earlier.
  (Almost ruled out)

- Oscillation (periodic pattern)

  ⇨ Not seen in the test setup yet.
  (Environment in/around hall 5 and hall west/magnet is different. But in the magnet oscillation was observed with only one card and without readout connection.)

- Noise (distorted pattern)

  ⇨ Most important issue for now.

  - Some preliminary study has been done. Trying to understand if there is any contribution from LV, HV and FED system to the observed noise and any correlation among them.
    (Nothing clear yet)

  - The grounding scheme (Analog, Digital and HV) in the chamber/pad plane has to be improved.

A. Mohapatra

9.11.00

S. SHULAL

ECAL Upgrade Status Nov.9 - 2000

1. Inner HV system

Production of 20 Inner HV distributors	**Done (almost)**
(MAX5250 chips are expected in December)	
Production of 70 on-module distributors	**Done**
Modification of CW bases	**Done 50%**

2. Noise suppression

Modification of CW bases	**Done 50% of Inner**

3. LED regulated LV supply	**Done**
4. Cables (repair and replacement)	**No**
5. Inner Module test for rad. damage	**Problematic**
Possibility: use Co source (0.2 mCi needed)	**???**
6. LED system distributor modification	**to be done in Dec.**

ECAL ELECTRONICS PLANS

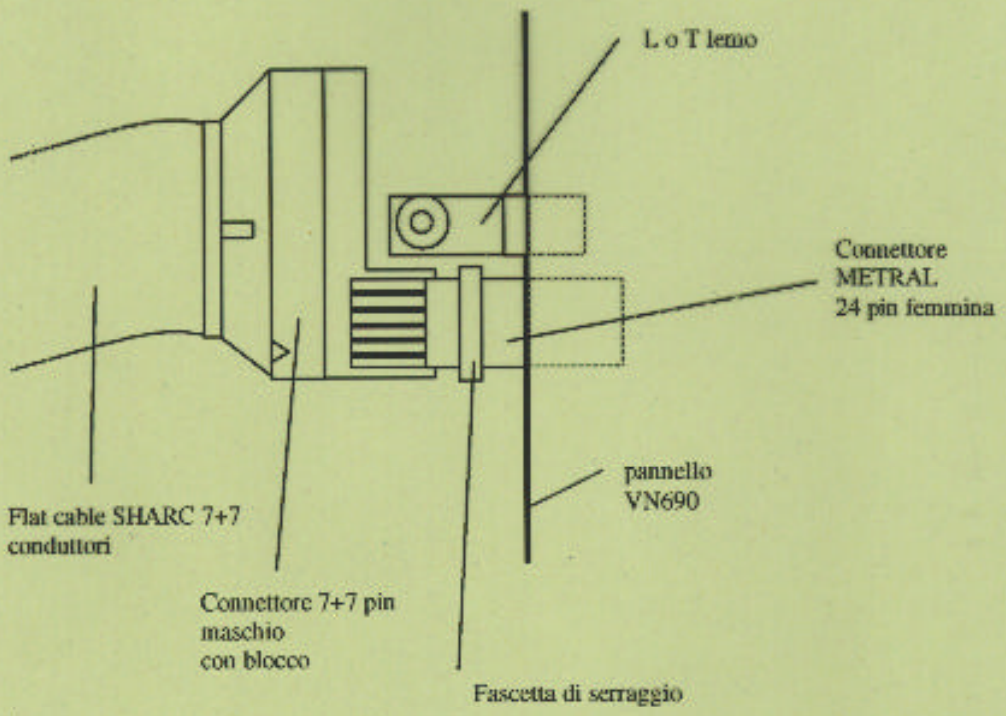
STATUS

READOUT

15/11 – 10/12 : • DISMOUNT BOARDS

- SEND ANALOG CARDS FOR MODIFICATION
- CHANGE SHARC CABLE CONNECTORS

PRETRIGGER : Brem. Recovery → DECEMBER 2000



Schema di climping del cavo SHARC (Visto dall'alto)

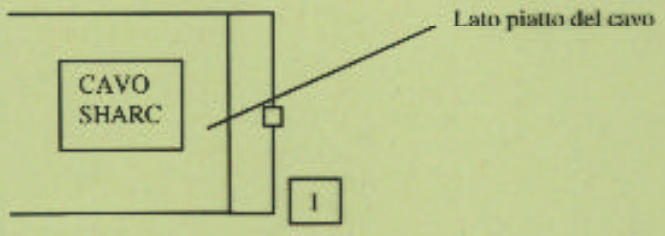


Tabella di corrispondenza connettore 7+7 (flat) e connettore METRAL

	6	5	4
D	8	4	5
C	7	3	6
B	10	12	14
A	9	11	13

NOTA : la coppiola 5-6 (CLK) è invertita

Segnali corrispondenti

	6	5	4
D	D3	ACK	CLK
C	/D3	/ACK	/CLK
B	D0	D1	D2
A	/D0	/D1	/D2

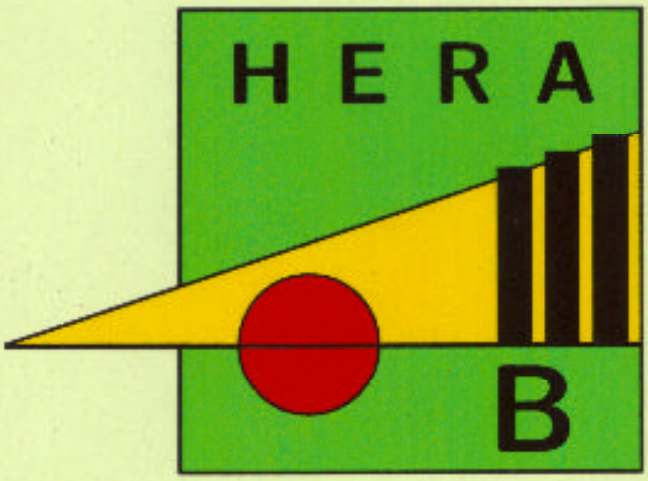
Universität Dortmund
Experimentelle Physik V

HERA-B Technical Board Meeting

DESY, Hamburg

November 9, 2000

Muon Pretrigger Status Report



for the Muon Pretrigger Group:

Ulrich Husemann

Experimentelle Physik V

Universität Dortmund

HERA-B

Universität Dortmund
Experimentelle Physik V

Pretrigger Link Board (PLB)

- 100% of the PLBs (40 boards) were installed during the run
- 36 PLBs **removed** after end of run and shipped to Dortmund for modifications
- 4 PLBs still installed for tests
- modifications:
  - **NO** changes in design
  - **mechanical fixations** of optical transmitters (piggy backs)

  → modifications **finished**!
- plans:
  - **tests** starting in November 2000
  - **re-installation** in May 2001

HERA-B

Experimentelle Physik V

Pretrigger Coincidence Unit (PCU)

- 100% of the PCUs (34 in pad system, 4 in pixel system) were installed during the run
- pad system:
  1 PCU with two defect channels and 3 PCUs with broken drivers shipped to Dortmund
  → debugging and replacing of drivers **finished**
- pixel system:
  2 PCUs and 4 Pixel Mapping Boards (PMBs) shipped to Dortmund
  → reprogramming of FPGAs, debugging, tests
- plans:
  - set up **test facilities** for PMBs
  - test and debug PMBs
  - further tests of pretrigger chain in pixel system

  → starting in **November/December 2000**

HERA-B

Experimentelle Physik V

Pretrigger Optical Link (POL)

- **hard work** to get stable running conditions
- measure stability by measuring **time without errors in control bit sequence**
- status during run (264 links in pad system):
  - ≈ 252 links: 0 errors in $t > 83\,\mathrm{min}$
  - ≈ 3 links: $83\,\mathrm{min} > t > 8\,\mathrm{min}$
  - ≈ 3 links: $8\,\mathrm{min} > t > 50\,\mathrm{sec}$
  - ≈ 6 links: $t < 50\,\mathrm{sec}$
- plans:
  - further **in-depth tests** of link behaviour

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Experimentelle Physik V

Muon Pretrigger Efficiency

- source: **detailed comparison** MUPRESIM – data
- overall number for 2000 run: $\epsilon = 92\%$
- **discrepancy** between $+y$ and $-y$
  (runs $17042, 17044$ but **not** run 15424):
  - working channels in $+y$: $\epsilon = 95\% - 98\%$
  - working channels in $-y$: $\epsilon > 99\%$
- **self-consistency check** of pretrigger messages:
  - momentum estimation: $p = p(r) = p(\xi, \eta)$
  - plot $r(p)$ vs. $r(\xi, \eta) \rightarrow$ bad correlation in $+y$!
  - BUT: LUTs used in data talking **o.k.**

  $\rightarrow$ study on **bit level** needed!
- **sources** of bit errors (calculate **XOR** of message bits):
  - rows ± 30: **geometry** problem
  - η: only **least significant** bits (physics effect?)
  - ξ: **all** bits affected (mean number: 5)

  $\rightarrow$ most likely: ξ **corrupted** in trigger chain

HERA-B

Technical board meeting
November 9th, 2000
DESY Hamburg

Progress and plans of the FLT

Imma Riu (DESY Hamburg)
On behalf of the FLT group

Outline:

- Software status
- Analysis status
- Hardware status

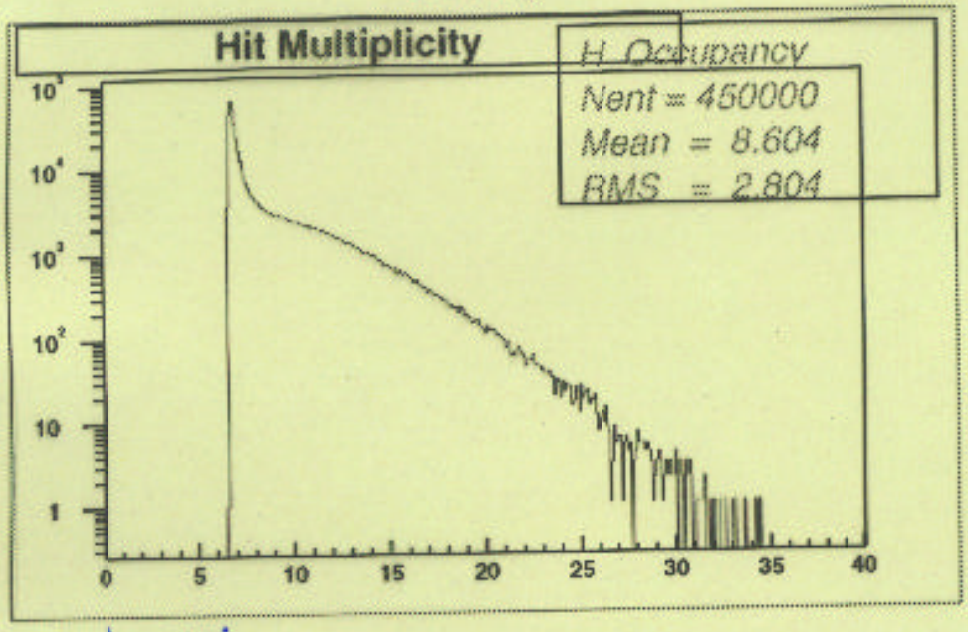
Software

	Status
FasSim implementation into ARTE	Finished
Online Link masking in FasSim	Finished
Msg. timing (latency) in FasSim	Finished
Masking of hot/dead WM channels in FasSim	Ongoing
Upgrade of the online software	Ongoing
FLT database	Started
ITR and muon pixels mapping	Spring 2001

Minimum Bias Events

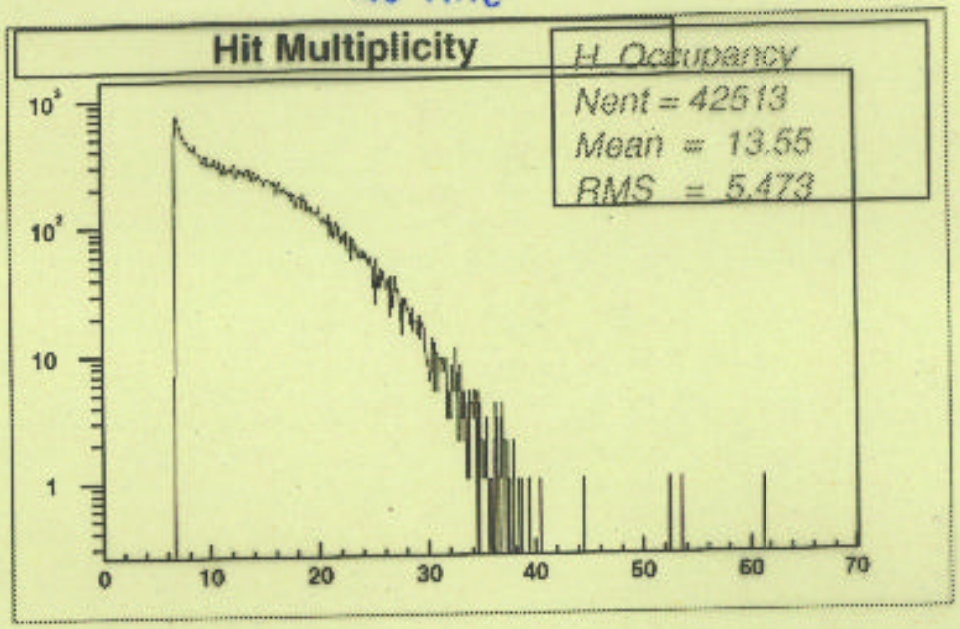
Holger Fleckenstein

5 MHz



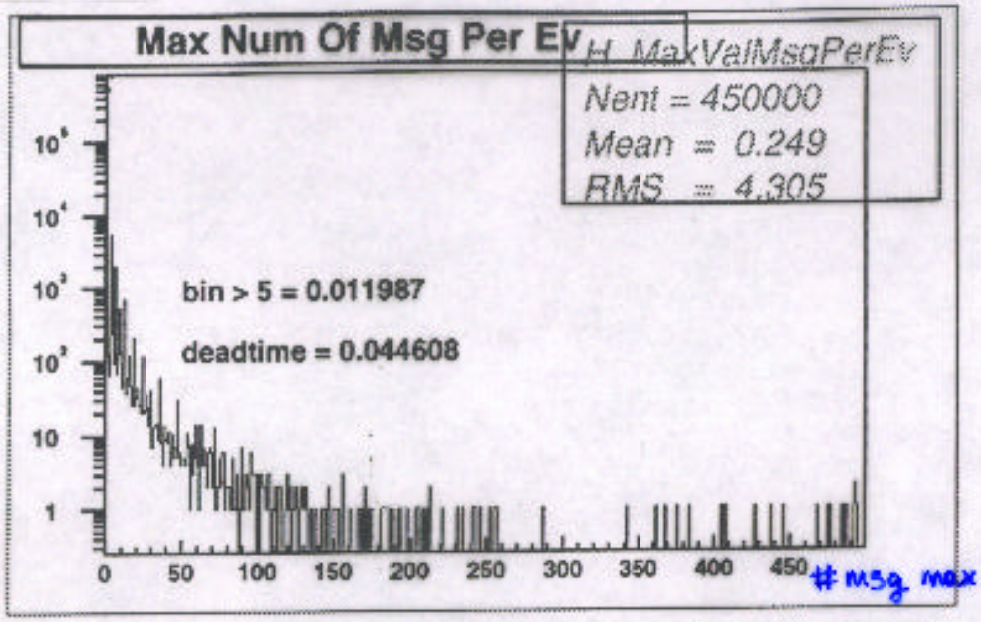
Due to link masking

20 MHz



Minimum Bias Events

5 MHz



5 msg. can be processed per event

⇓

TFUs with # msg > 5 are producing pile-up.

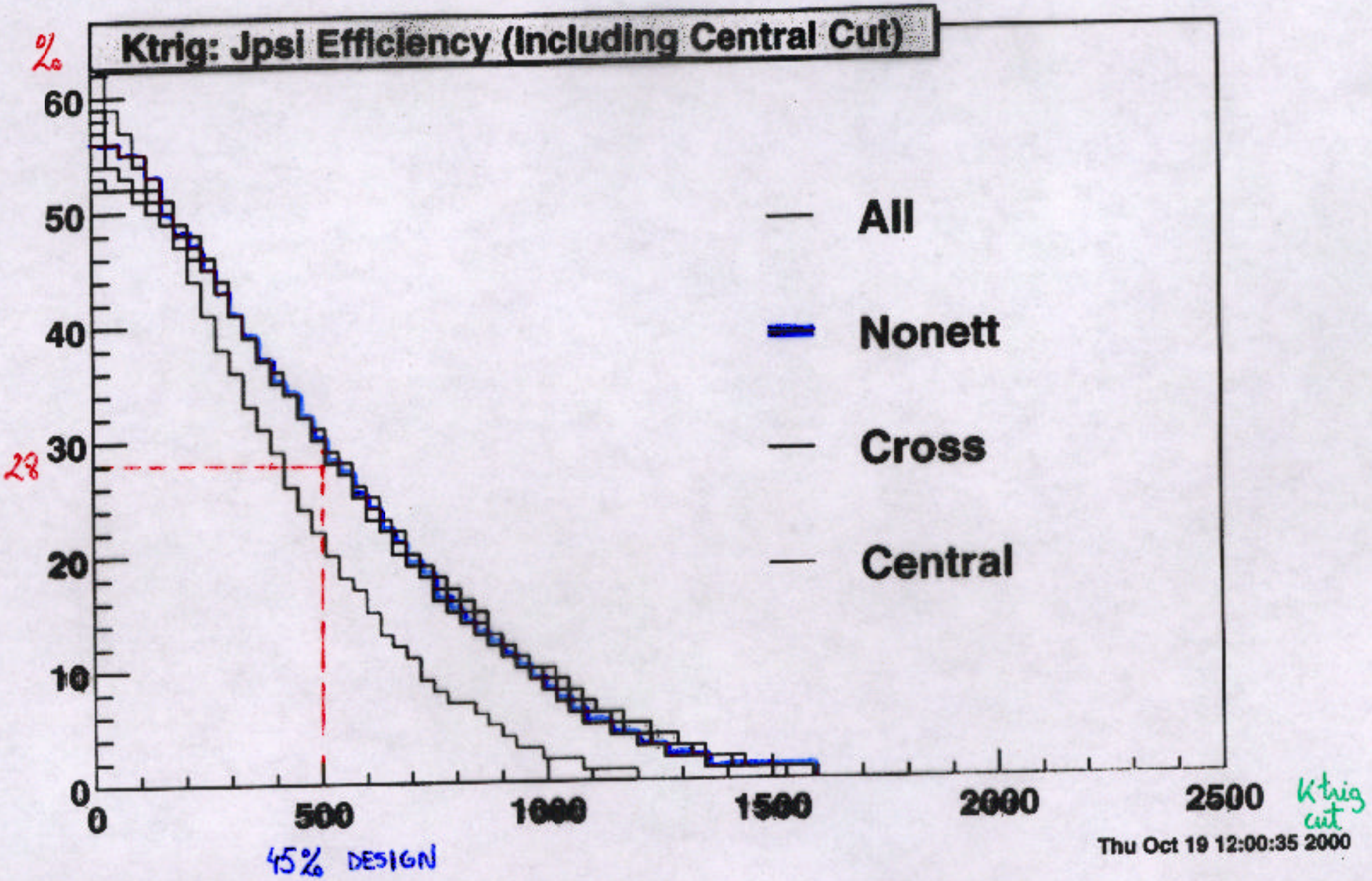
Deadtime = # events affected by this pile-up.

(IS AN UPPER LIMIT)

Analysis

	Status
Efficiency of Geo., ktrig>500	Finished
Understand online/offline discrepancies	Ongoing
FLT Muon track efficiency	Ongoing
Understand MU1 inefficiency	Started
Understand FLT rates	Start soon
Understand/improve latency	Start soon
Improve FLT tracking	Spring 2001

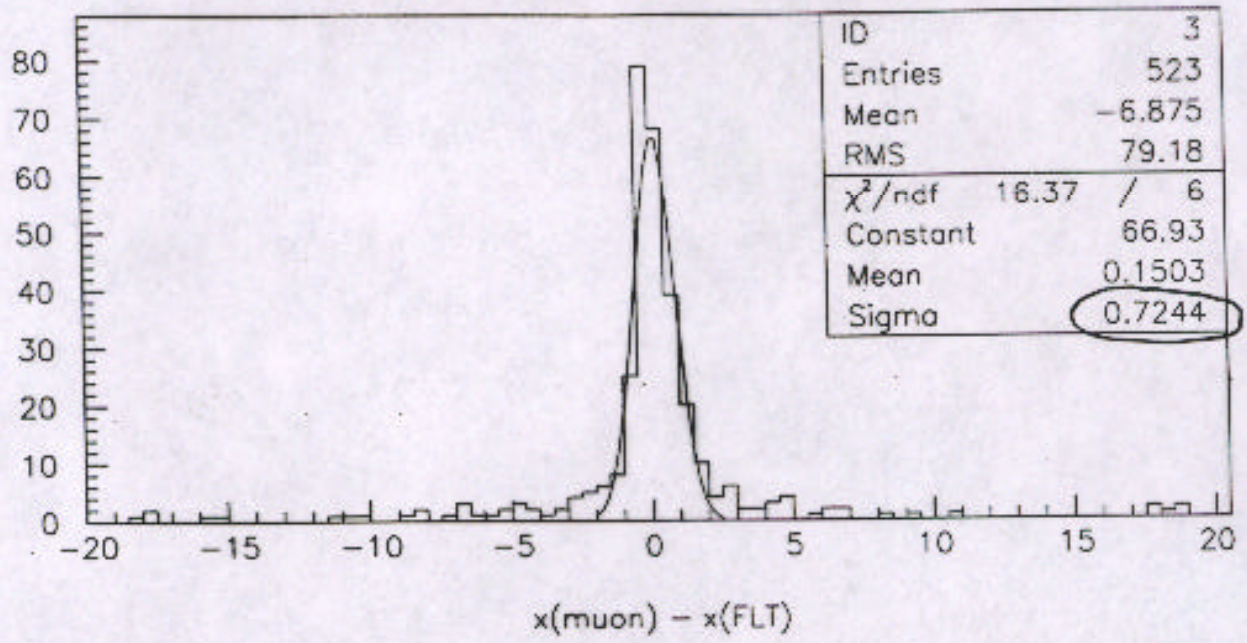
Joachim Flammer

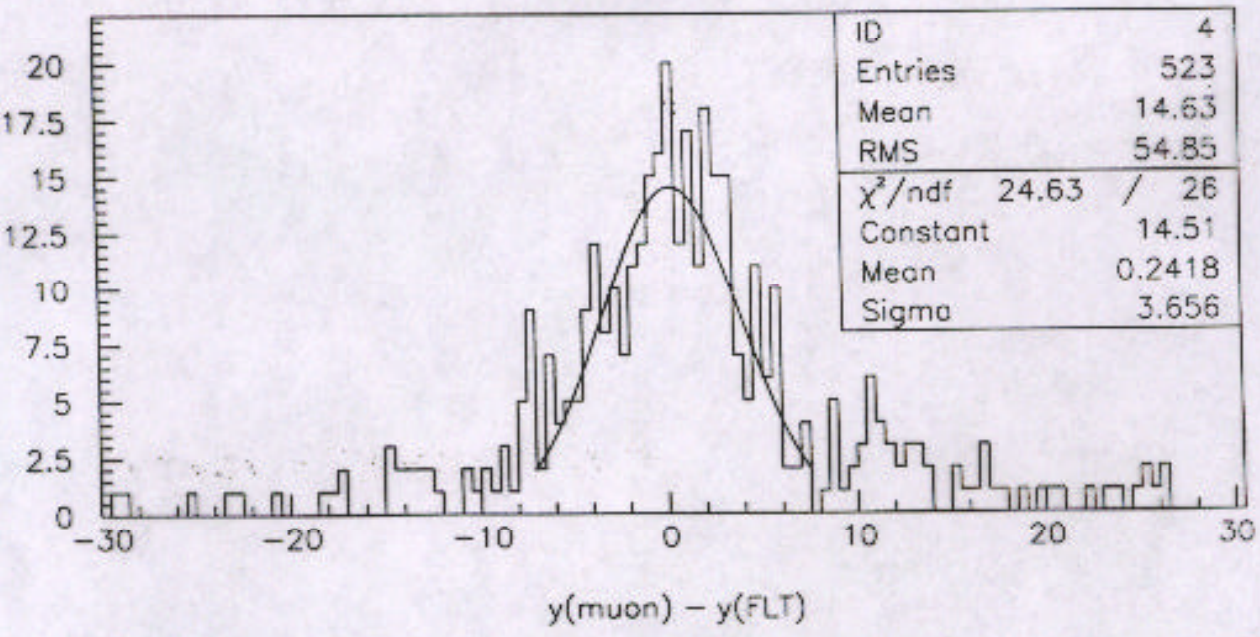


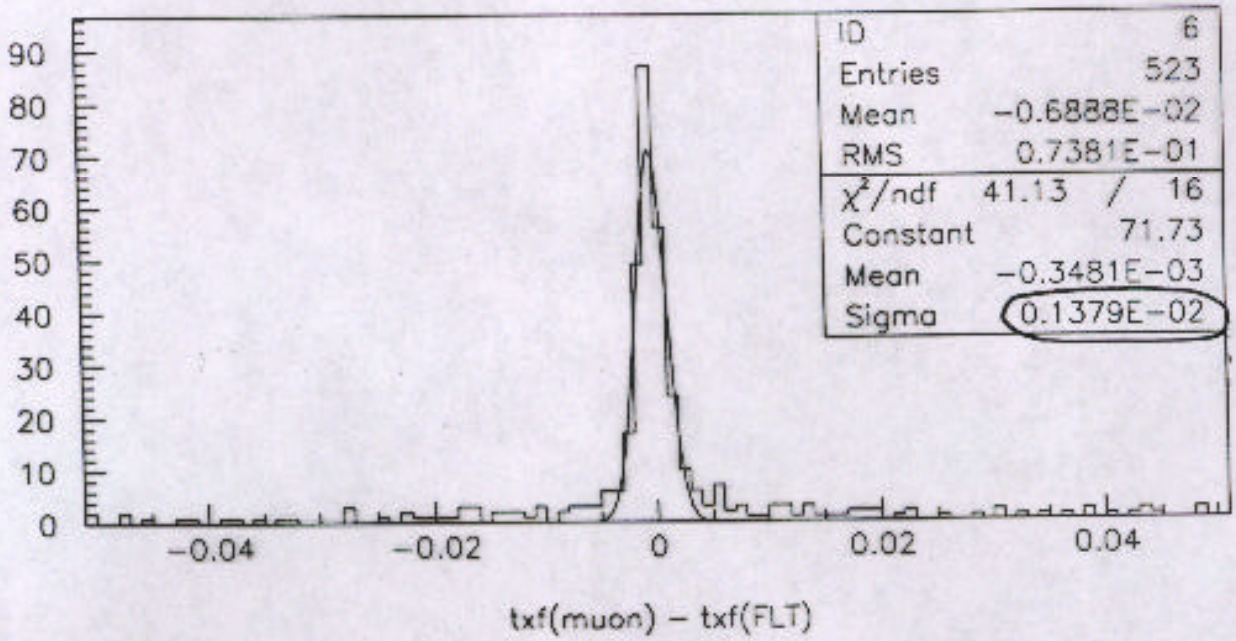
Alexander Somov

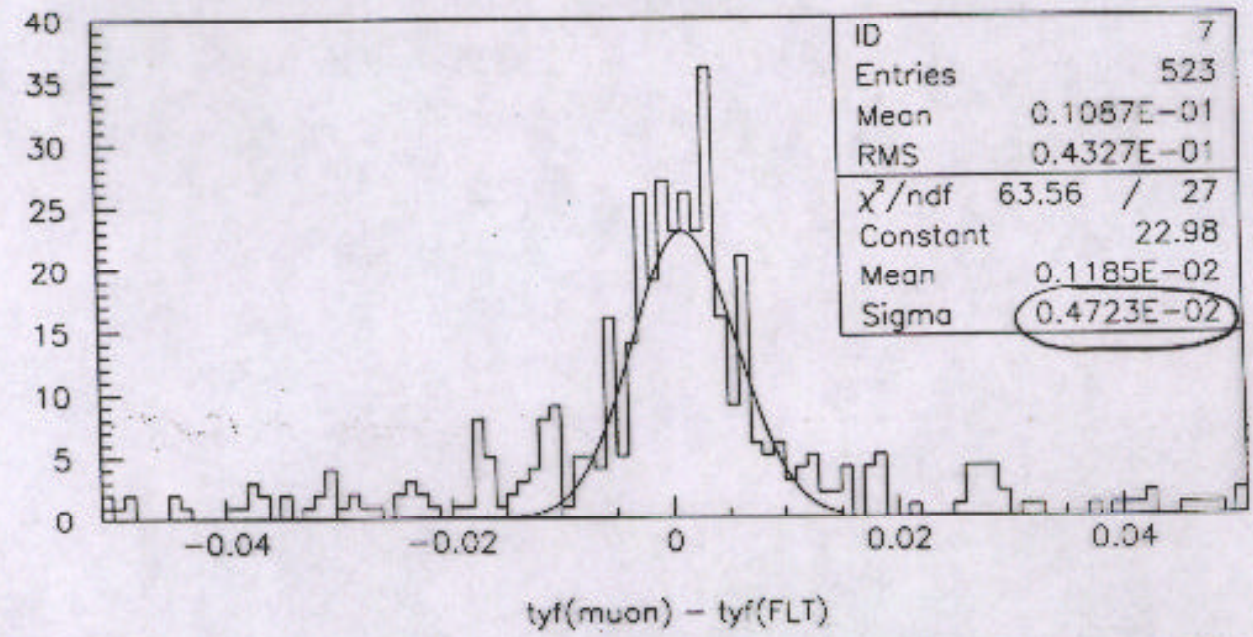
MUON EVENTS

MUON REF TRACK – MUON FLT









- REF MUON TRACKS ARE BIASED TOWARDS FLT TRACKS BECAUSE THEY ARE BUILT USING THE MUON SLs AS FLT DID.

- A LIKELIHOOD PROBABILITY IS CALCULATED. DEPENDING ON THE CUT:

$$\epsilon_{ff} = 19\% - 40\%$$

Hardware

LINKBOARDS	Availability	Schedule	Effort
Set offset to trasmitter by software	√ MA	**Spring 2001**	**Big**
Mecanical support for better cabling		**In discussion**	**Big**
Possibility of event-by-event comparison		December 2000	Ok
New software for LB programming	×	?	?
TFU related			
Heat exchange in trailer	√	Finished	–
Better TFU receivers	√ MA	December 2000	Ok
Better repeaters (reset & less errors)	√ MA	**Spring 2001**	Ok
Better msg. boards (error count)	√ MA	December 2000	Ok
Better msg. MUX PECL to LVDS	√ MA	**Spring 2001**	Ok
Possibility to ommit one hit in TFU	√ MA	–	**FasSim**

SLT tasks

SLT task	*Responsability*	*Status*	*Priority*
ITR-integration	DESY-HH (HD-ITR)	Started	Now
RoI-based sparsification			
Finalize CnA loading code			
Testing ITR-SLT code			
L2-Magnet	NBI	Advanced	Long term
Inclusion of the ITR			
Testing			
Refit	DESY-HH		
Drift-Time		Not started	Soon
Timing optimization		Started	Long term
L2Sili	NBI	Started	Long term
Code improv. (mult. scatt.)			
L2Vertex	NBI	Advanced	Long term
Trigger decision			
MC-DAQif	DESY-HH		
Digit-OTRi/Drift-time		Advanced	Now
Digit-ITR (HD-ITR)		Not started	Now
Timing opt. and mapping	DESY-HH	Not started	Long term
MAP optimization			
RoI-Marvin (HD-VDS)			

SLT tasks (cont.)

SLT task	*Responsability*	*Status*	*Priority*
Trigger typ handling	DESY-HH	Started	Long term
DB information by CnA			
SLT code development			
SLT-2000 Analysis	NBI/DESY-HH	Started	Now
SLT track resolution			
SLT single track eff.			
FLT-SLT matching study			
SLT rejection/timing study			
J/Ψ rate drop in Aug 2000			
SLT-Arte support	NBI/DESY-HH		
sltinfo + tools		Advanced	Soon
MC-DSLT production		Started	Soon

Software status

Name	Status	Remarks	
SHARC			
SLB	needs improvement	low perfomance	A.Zhelezov
EVC	complete	more functionality	
SWITCH	complete	could be improved	F.Sanchez
UNIX			
RPM	needs improvement	threads, compression	V.Rybnikov
NAM	complete	name service crash	V.Rybnikov
PAR	complete		
EMG	complete		
PRC	complete, extension	remote nodes monitoring	J.Hernandes
CNA	complete		
PRCM	complete	small fixes	V.Rybnikov
RSM	needs development		V.Rybnikov
SMC	needs investigation	many clients	V.Rybnikov
RCDB	needs development	RCDB editor	A.Zhelezov
RHP	complete	(compression dor DB)	
FCS	complete	CAN-BUS readout can be included (not needed)	F.Sanchez
GUI	complete		

PCI to SHARC board driver for the new Linux kernel 2.2.14 — S.Esenov

V. RYBNIKOV

DAQ status

1. **DAQ is available (tested for MUON)**
2. **Reprocessing can be used**

New features:

- setting the paths for DST and MINI to be used by the robot for automatic data copying
- writing the number of terminated processes to the DB
- a new run parameter for distinguishing the interrupted reprocessing

SLT nodes status

Status	Quantity	Comments
Dead (don't switch on)	4	047, 057, 112,183
Problem with booting due to the wrong date/time setting	14	006, 051, 056, 057, 058, 064, 065, 068, 070, 072, 073, 074, 114, 182
No power indication (working well)	1	186

F. SANCHEZ

Fast Control System

Priority	Problem	Action
1.	Investigate problems with OPR and MOON FCS connections. Suspicion --> Optical transmition	Revive Can Bus FCS daughter readout. It checks the BX transmition & the error from Serial/Parallell.
2.	Improve latency of the FCS. The FCS is clocked with BX.	Look at schematics of FCS to understand protocol. Think about overclocking/protocol modification.
3.	Trigger priority (trigger mask). Consequtive triggers. Reprograming of logic via VME to speed up the debugging, functionality upgrades.	Looked at the protocol & be ready for mod. of priority 2.

WORKING SCENARIO

1. point should be fixed/understood @ the start up of the machine next year.
2. & 3. can be included afterwards (end 2001/begin 2002) in case it needs a mayor modification on the Hardware.

PS> MPI-HD is trying to find a diploma student to contribute to the FCS effort.