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Second and Third Level Trigger Systems for the HERA-B Experiment

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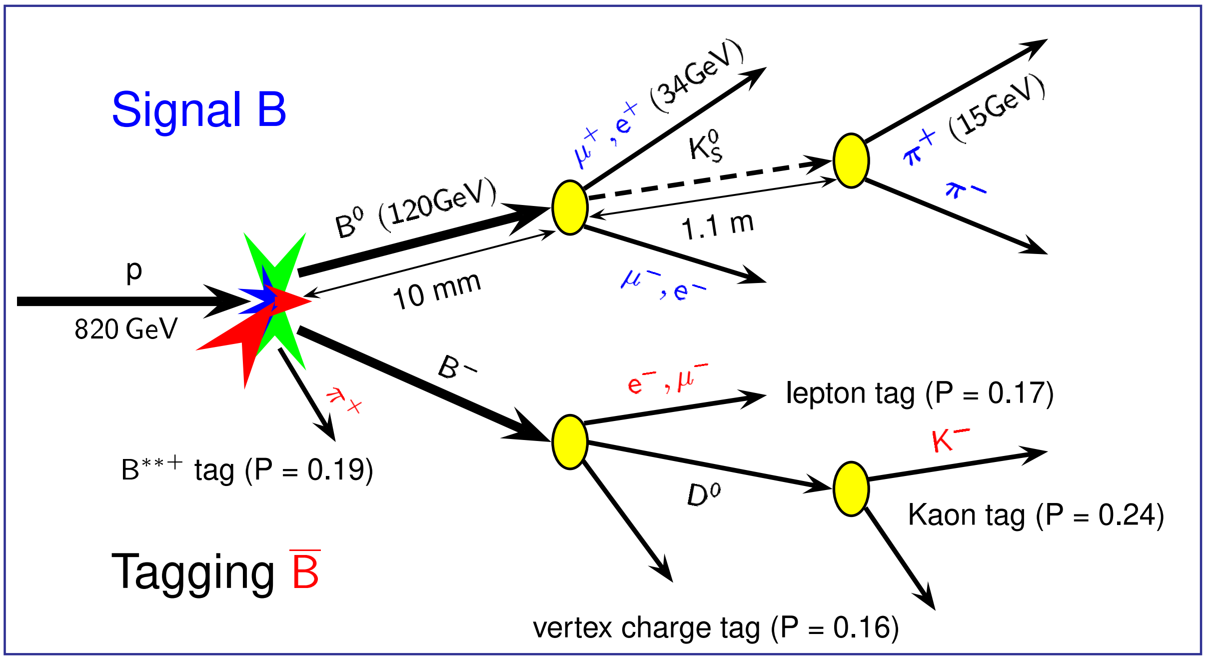
Principal Physics Goals

- **Observation of CP Violation, in**

$$B \longrightarrow J/\psi K_S^0$$

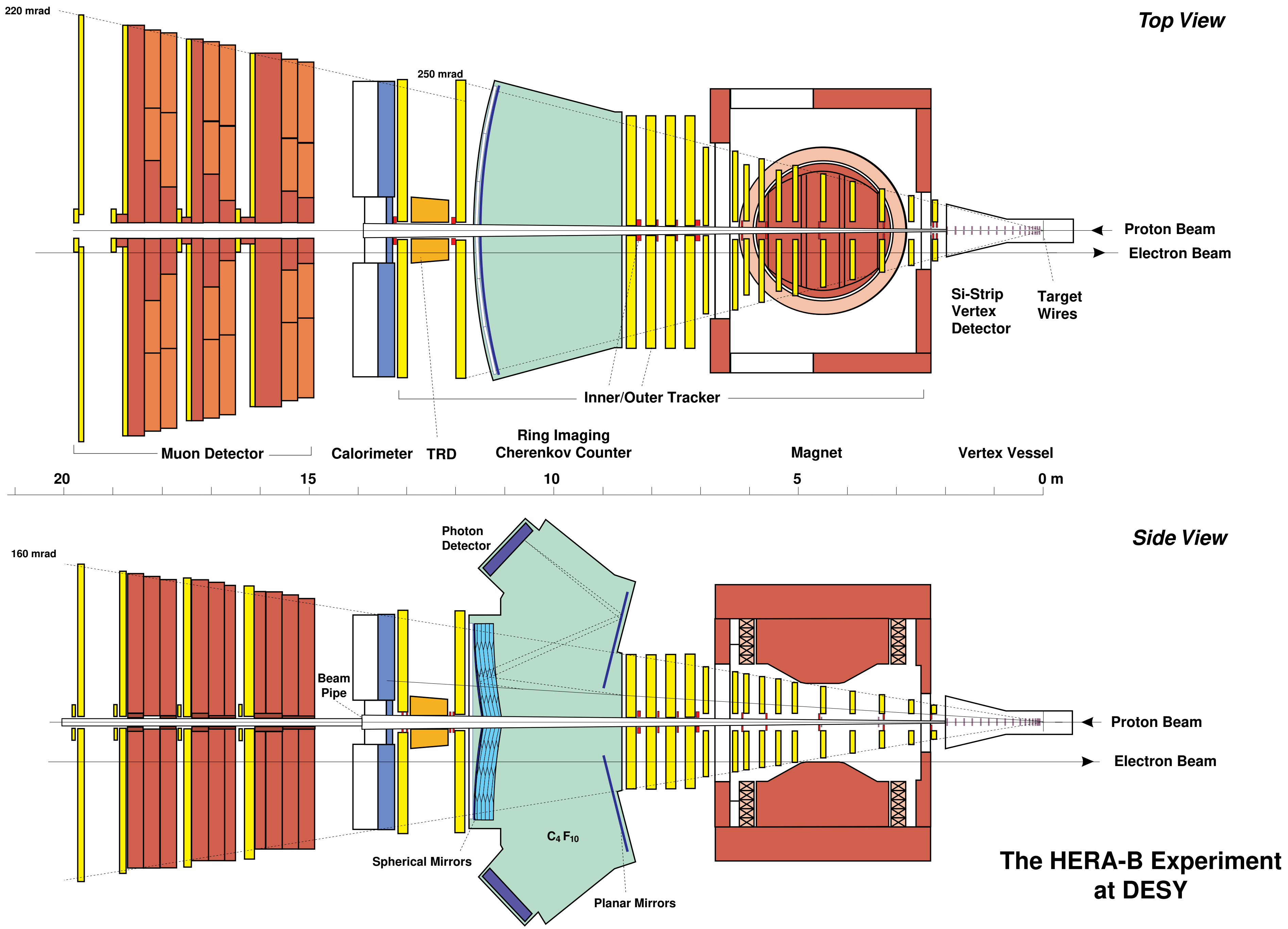
$$J/\psi \longrightarrow \ell^+\ell^-,\ K_S^0 \rightarrow \pi^+\pi^-$$



- **Observation of B_s Mixing, in**

$$B_s \longrightarrow D_s^{(*)}\ell\nu$$

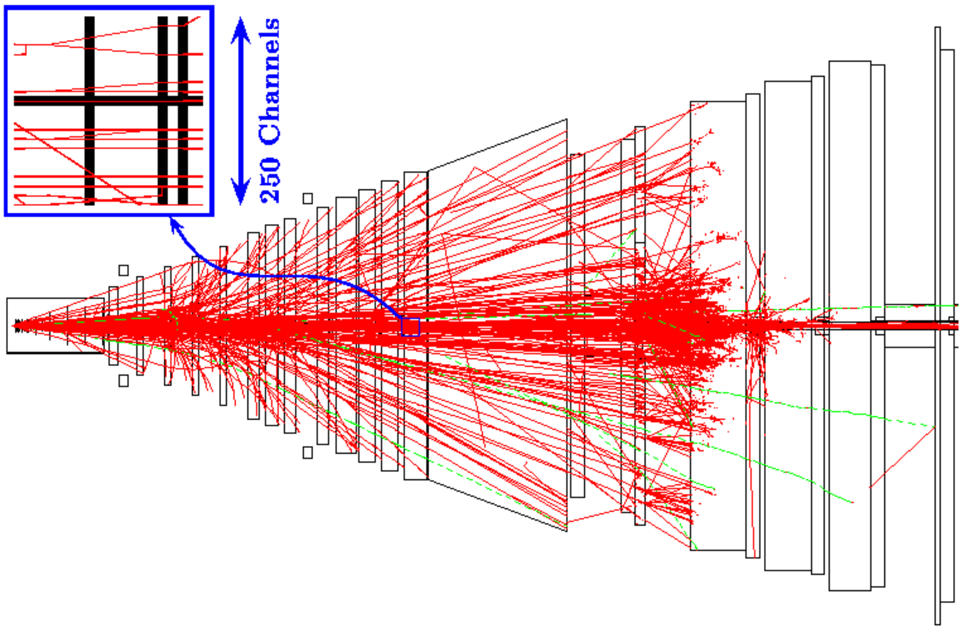
$$(b \longrightarrow \ell X)$$


Top View
220 mrad
250 mrad
Proton Beam
Electron Beam
Si-Strip
Vertex
Detector
Target
Wires
Inner/Outer Tracker
Muon Detector
Calorimeter
TRD
Ring Imaging
Cherenkov Counter
Magnet
Vertex Vessel
20
15
10
5
0 m
Side View
160 mrad
Photon
Detector
Beam
Pipe
Proton Beam
Electron Beam
$C_4 F_{10}$
Spherical Mirrors
Planar Mirrors
The HERA-B Experiment
at DESY

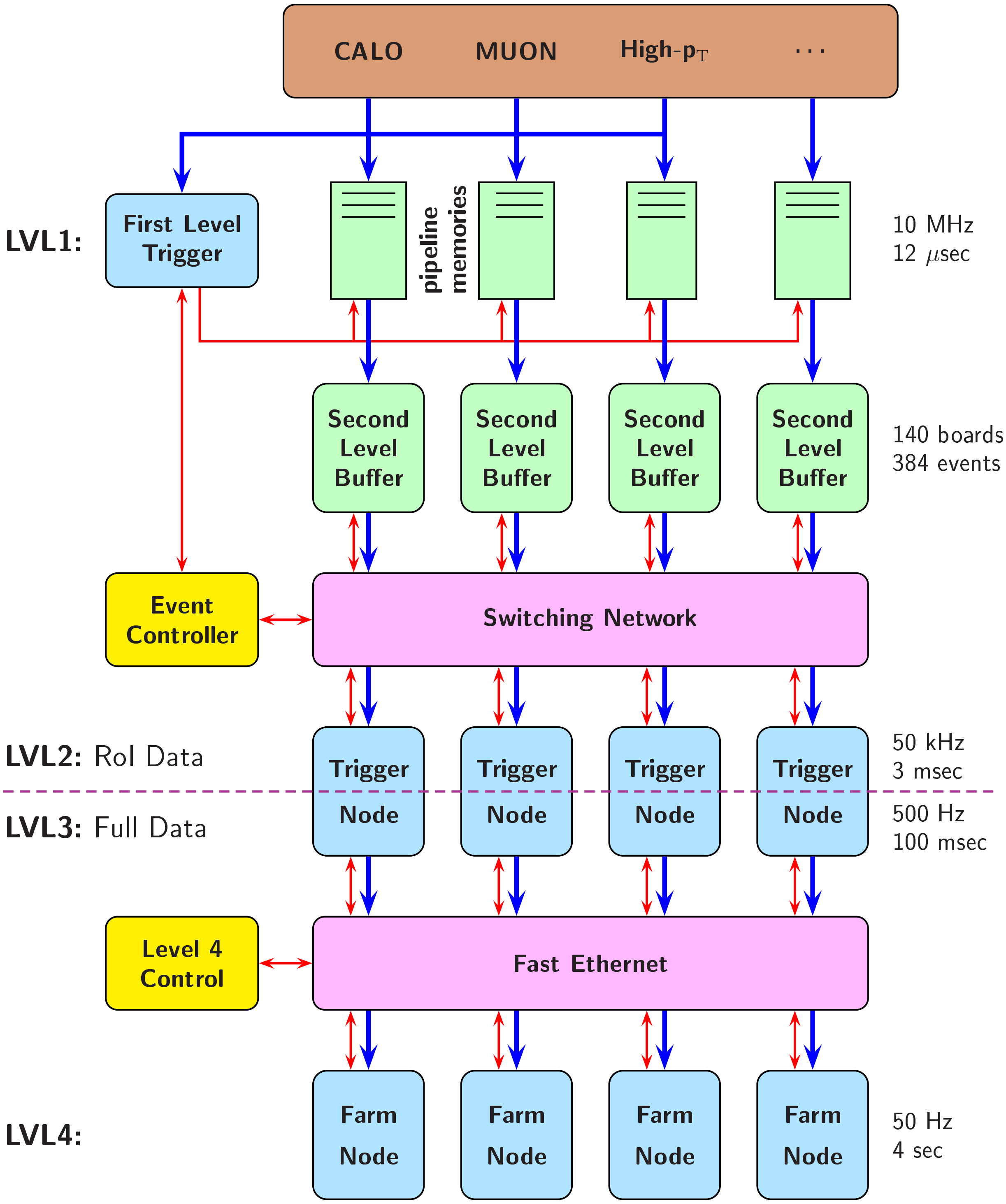
Operating Environment

- Signal / Background: $\approx 10^{-9}$ to 10^{-11}
- Bunch crossing rate: 10 MHz
- Mean # interactions per crossing: 4
- Rate of interesting signals: $\ll 1$ Hz
- Mean track multiplicity / crossing: 120
- Detector occupancy: Up to $\approx 20\%$

A typical event with 4 interactions:



Trigger System Architecture



Trigger Overview

Stage	Time Scale	Input Rate	Input Data [Mbyte/sec]
Pretrigger Define **RoIs** (Regions of Interest) from - ECAL - Muon filter - High p_T pad chambers	1 μsec	10 MHz	90,000
Event data in Level 1 Pipeline		↓ 1/1	
Level 1 - Find tracks behind magnet inside RoIs - Two particle mass cut or p_T cut	12 μsec	10 MHz	10,000
Event data to Level 2 Buffer		↓ 1/200	
Level 2 Re-find and refine Level 1 tracks: - more chambers, drift time, compute χ^2 Tracking through magnet and silicon. Require detached vertex or impact parms.	3 msec	50 kHz	250
Full event data to Level 2/3 Farm		↓ 1/100	
Level 3 Silicon reconstruction on full event data. For impact parameter triggers, search for other tracks forming secondary vertex.	100 msec	500 Hz	250
Event data to Level 4 Farm		↓ 1/10	
Level 4 - Full event reconstruction. - Classification. - Monitoring and calibration.	4 sec	50 Hz	6
Event data to mass storage		↓ 1/2.5 20 Hz	

The Scale

- channel count: 500,000
- event size (uncompressed): 500,000 bytes
- event size (compressed): 120,000 bytes

Data flow [Mbytes/sec]	
➠ L1 pipeline	5,000,000
➠ L2 buffers	25,000
➠ L2/L3 processors	500
➠ L4 processors	6
➠ Tape	2.4

L2/L3 Architectual Details

Event Controller hands full responsibility to processing node for a given event.

Processing node **pulls** more and more data from buffers as needed:

Level 2: Until decision is reached

1) Tracking chambers x
2) Tracking chambers y
3) Magnet chambers
4) Silicon Vertex Detector

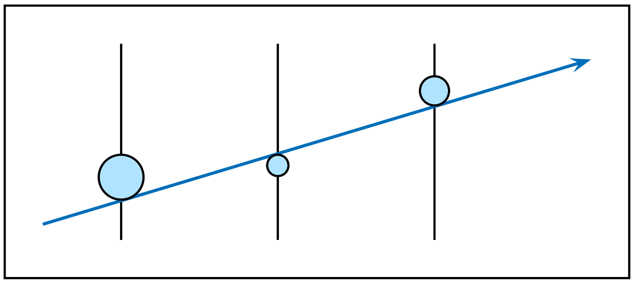
Level 3: Full event data

- Event building
- Level 3 filtering

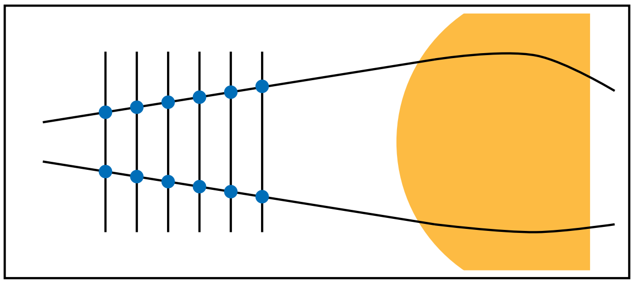
L2/L3 Algorithm

Level 2 (RoI based)

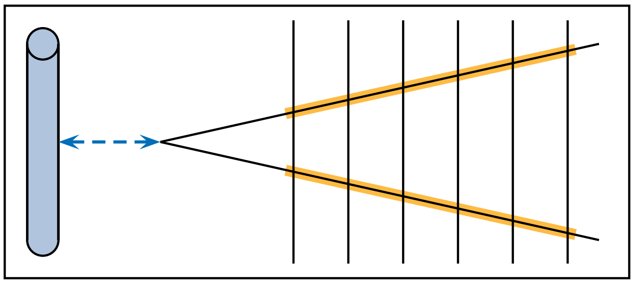
- Refine L1 tracks:
  - add chambers
  - drift times
  - χ^2 cut



- Traverse magnet and perform tracking through silicon vertex detector

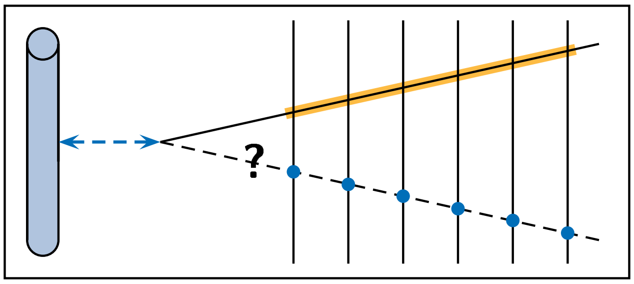


- Require detached vertex or two tracks with non-zero impact parameter



Level 3 (Full Data available)

- Search silicon for other tracks forming detached vertex with L2 impact parameter tracks



Data Path Components

- SHARC cluster board
  170 units, 1000 DSPs
  - Level 2 buffers
  - Fast switching network
  - Control

- Pentium II processors (300 MHz and higher)
  400 units
  - L2/L3 trigger farm: 200 units
  - L4 trigger farm: 200 units

- SHARC/PCI interface card
  200 units
  - Bridge: L2 buffers $\leftrightarrow$ processors

- Fast ethernet
  - Level 3 $\leftrightarrow$ Level 4 connection
  - Some control functions
    (booting, initializing, . . .)

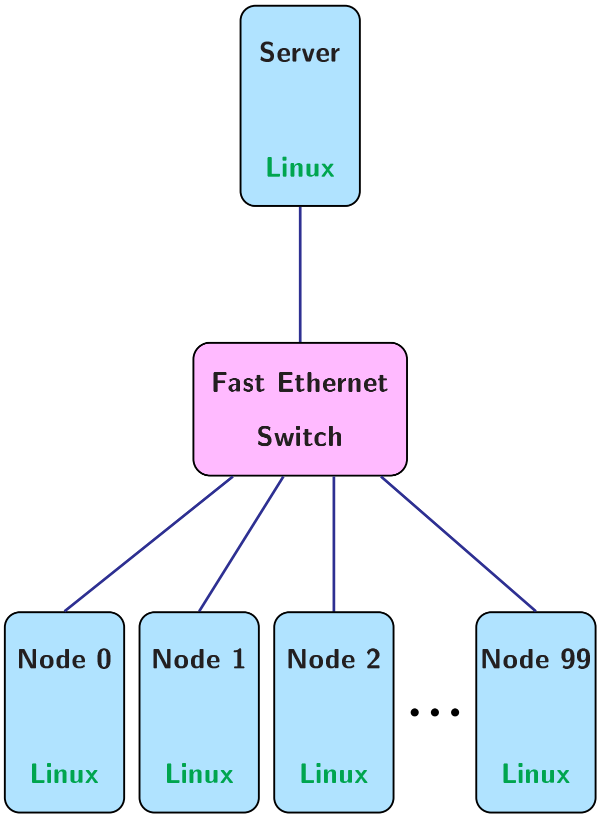
L2/L3 Farm Node

Standard Personal Computer equiped with:

- Off the shelf components
  - Pentium II Processor, 300 MHz
  - 64 MB SDRAM
  - Floppy drive
  - Cheap graphics card
  - 100 Mbit/sec Ethernet adapter
- Custom made components
  - Sharc–to–PCI Interface
    - Throughput: $\sim$ 40 MByte/sec
    - Latency: < 1 μsec
  - Slow control interface (CAN protocol)
    - Power up/down and reset PC
    - Measure temperature and voltage
    - Automatic shutdown in case of overheating

L2/L3 Farm

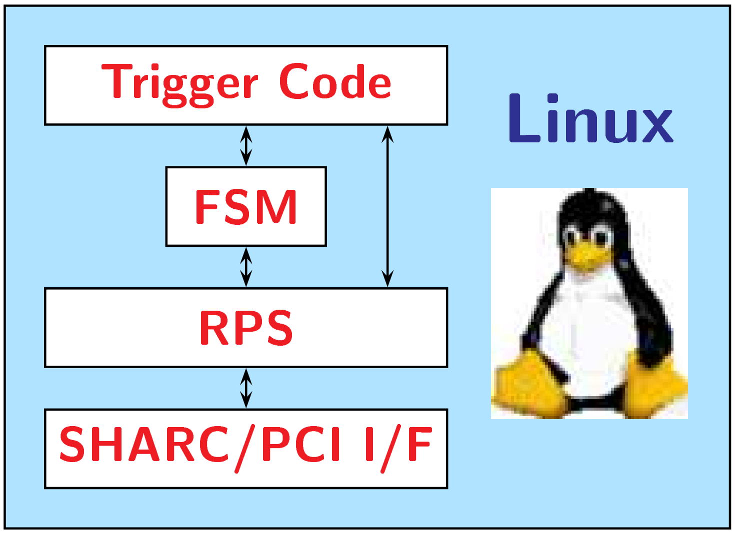
100 nodes already installed



Booting and Control:

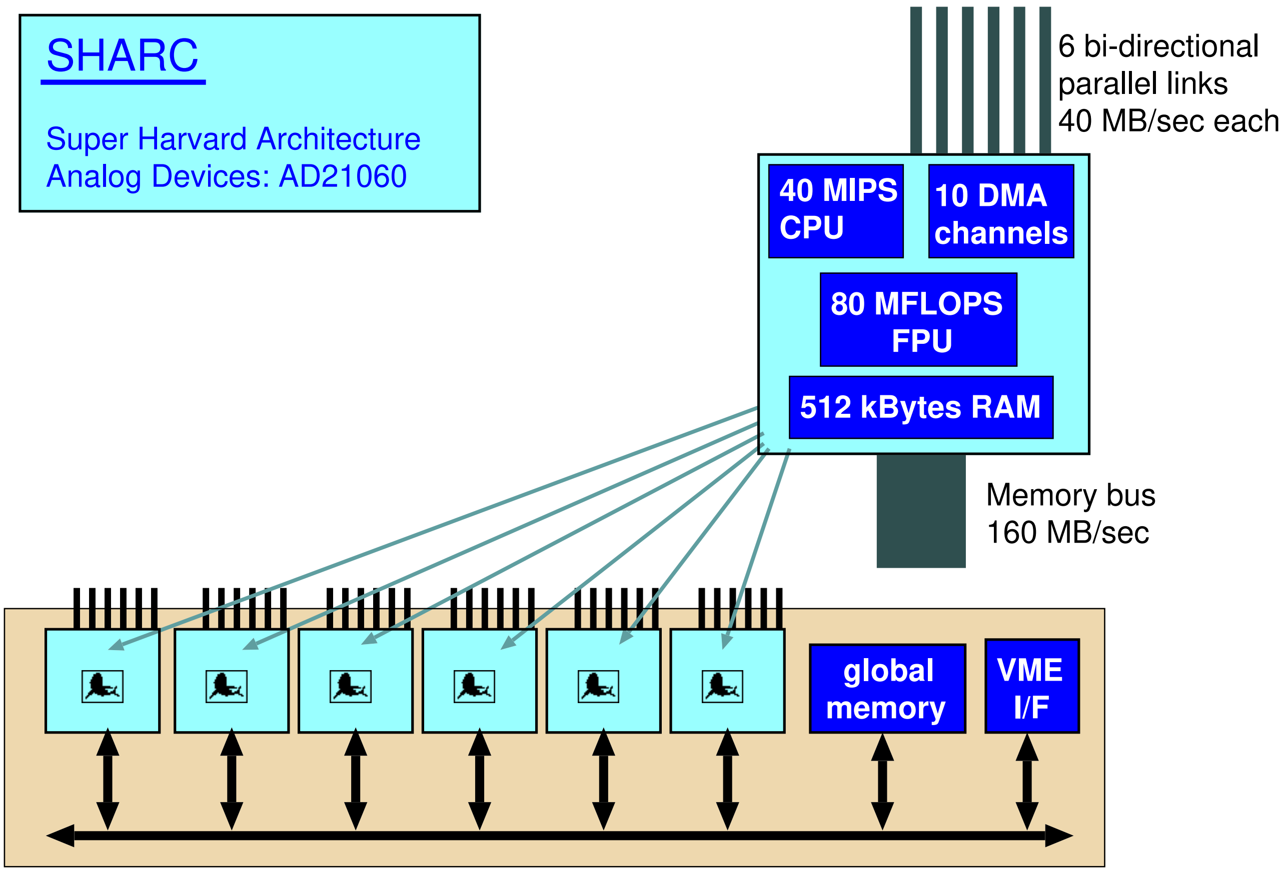
- Linux Boot/Root from floppy
  (experimenting with Ethernet boot)
- IP address from server via BOOTP
- NFS mount executable(s) from server
- Remote process control via local server process

Trigger node software environment



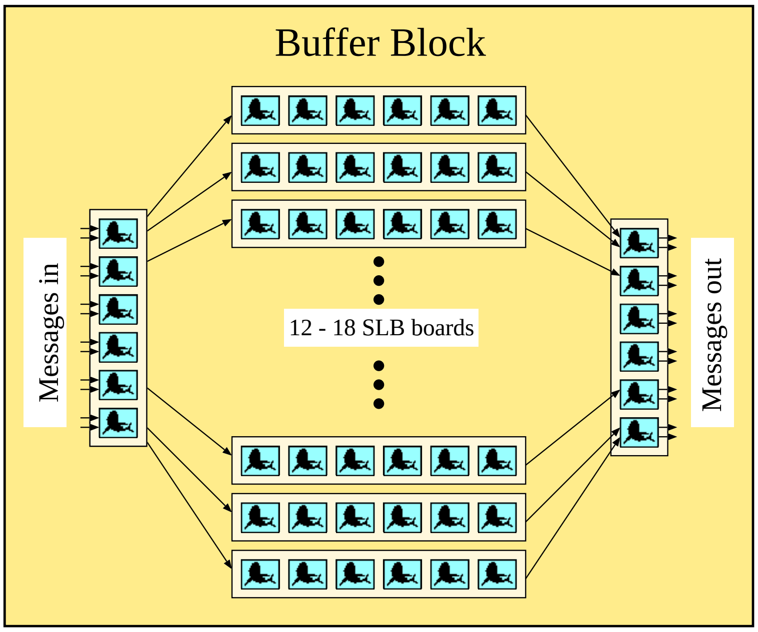
- Linux operating system
  Pruned down system: boot from floppy
- Only essential processes run.
  Keep only trigger process active.
  $\Rightarrow$ avoid context switching!
- Message driven trigger: polling protocol.
- Non-standard I/O driver copies data directly between sharc link i/f and user space
  (overhead $< 1\mu$sec)
- FSM: finite state machine for run control
- RPS: routing service for sharc link.

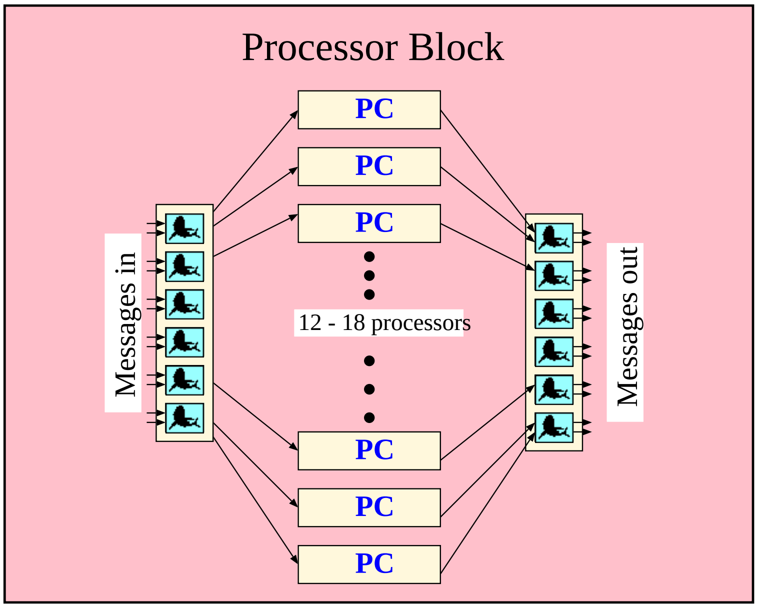
SHARC cluster board



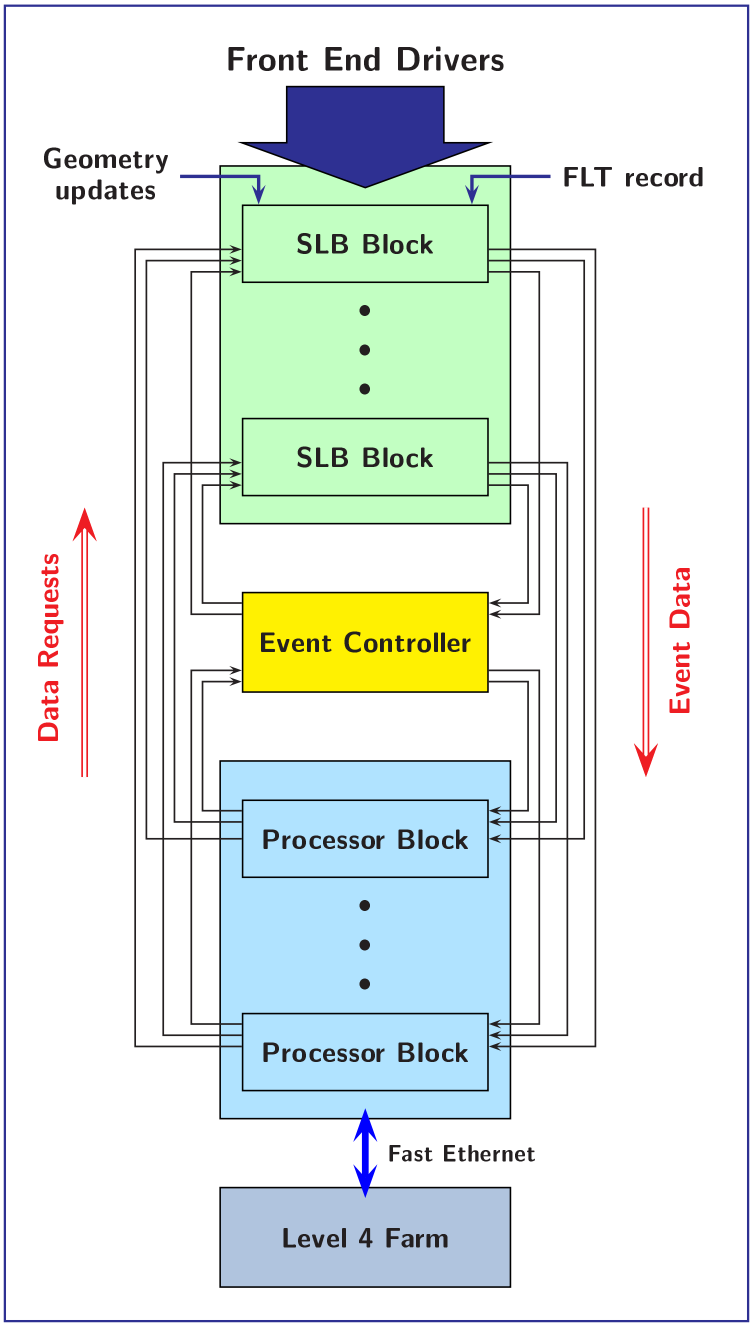
- 6u VME card
- All 36 links available on front panel
- Producer: MSC, Sutensee, Germany

Network Building Blocks





Topology



SLT $\Leftrightarrow$ proc. dialog:

12 ‘hops’ round trip, 5μs per hop $\Rightarrow$

60μs roundtrip time for zero length message.

1998 Run

Detector status; fraction ready for 1998 run:

- Silicon Vertex Detector 1/4
- ECAL incl. read-out 1/2
- RICH 1/1
- Muon Chambers 1/3
- + modules from all other subsystems

Trigger chambers missing:
Base trigger on ECAL hits and silicon matching

Starting rate (1 interaction / crossing): 8 MHz
Level 1: Two high p_T ECAL hits $\rightsquigarrow$ 10 kHz
Level 2: Di-electron mass cut;
Silicon tracking/vertexing $\rightsquigarrow$ 100 Hz

Complication: No RoI information from Level 1. Level 2 has to search complete ECAL.

Level 2 Hardware: 100 processor nodes, 50 buffer boards, switch.

October: Integration of full data path.

Physics program: J/ψ production and $\sigma_{b\bar{b}}$.

Status & Plans

- Trigger hardware for 1998 run exists and is being installed.
- All essential software components exits.
- Full DAQ/trigger chain to be commisioned this autumn on sizeable system.
- 1999: Full system.