Triggerscheme for the HERA–B Counting Rate Experiment 1998

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In general a triggersignal indicates interesting events and is needed to start the electronic that monitores these events. It represents a connection between the electronic and the Data Aquisition (DAQ): Signals that are created by the trigger are needed to steer the different electronic modules.
In our case, signals are fed into different electronic modules like Scalers, ADC's, TDC's and FADC's. In addition one must be able to stop and prepare the modules for the next event. Therefore one don't need a triggersetup that only generates a triggerpulse, but also generates the steering pulses for the modules. The used triggermodules in rack number 5, NIM–Crate 3 are shown in figure 1.

1	2	3	4	5	6	7	8	9	10	11	12
Logic FIFO 4x4	Coincidence Unit	Quad Gate Delay	Dual Timer	Quad Coincidence	Logic FIFO 2x8	Dual Timer	Level Adapter	Coincidence Unit	8 channel Discriminator	Dual Timer	Dual Timer
1BX	A&B = Trig C = Coinc	1BX-delay 500ns	READY FF	LAM & G1	READY & 0BX ADC-Gate TDC-Start	VME-Stop delay	NIM in TTL out VME-Stop	Coinc	 Puls 1 Puls 2	CAMAC Inh.-Gate 100 ns	RRT-Gate 220 x 96ns
LAM in $\overline{\text{LAM}}$ out	READY & Trig	READY-delay 100ns		READY & 0BX/Coinc				A = Coinc B = 0BX			
RRT		0BX-delay 50ns	CAMAC- READY FF	READY & 1BX	READY & 1BX TDC-Clear ADC-Clear	G1- delay	TTL in NIM out CAMAC-Inh.			G1-delay 1 ms	RRT-Gate 2200 x 96ns
READY	1BX & FF	1BX-delay 3000ns		G1 - OR							

Figure 1: *Electronic modules that are used for the trigger–setup in rack 5, NIM–Crate 3. The numbers show the accordant slot.*

The function of the trigger used in the experiments '98 DAQ is described in section 1. In general it works in the following way: When a signal appears while the first bunch crosses the target, a triggersignal will be created. This triggersignal starts the DAQ.
To use the trigger for calibration and testing of electronic modules, there exists a possibility to modify the trigger in such a simple way. This is described in section 2.

1 The ‘Event’–Trigger for the Counting Rate Experiment 1998

1.1 Principle

The triggerscheme of the ‘Event’–Trigger is shown in figure 2. The numbers appearing in this scheme belong to the accordant slot of the module as shown in figure 1. The numbers contain the rack number first, the crate number second and the slot third. E.g. one can find the 500ns delay unit **6–3–3** for the 1BX–signal in rack number **6**, NIM–Crate **3** and slot number **3**.

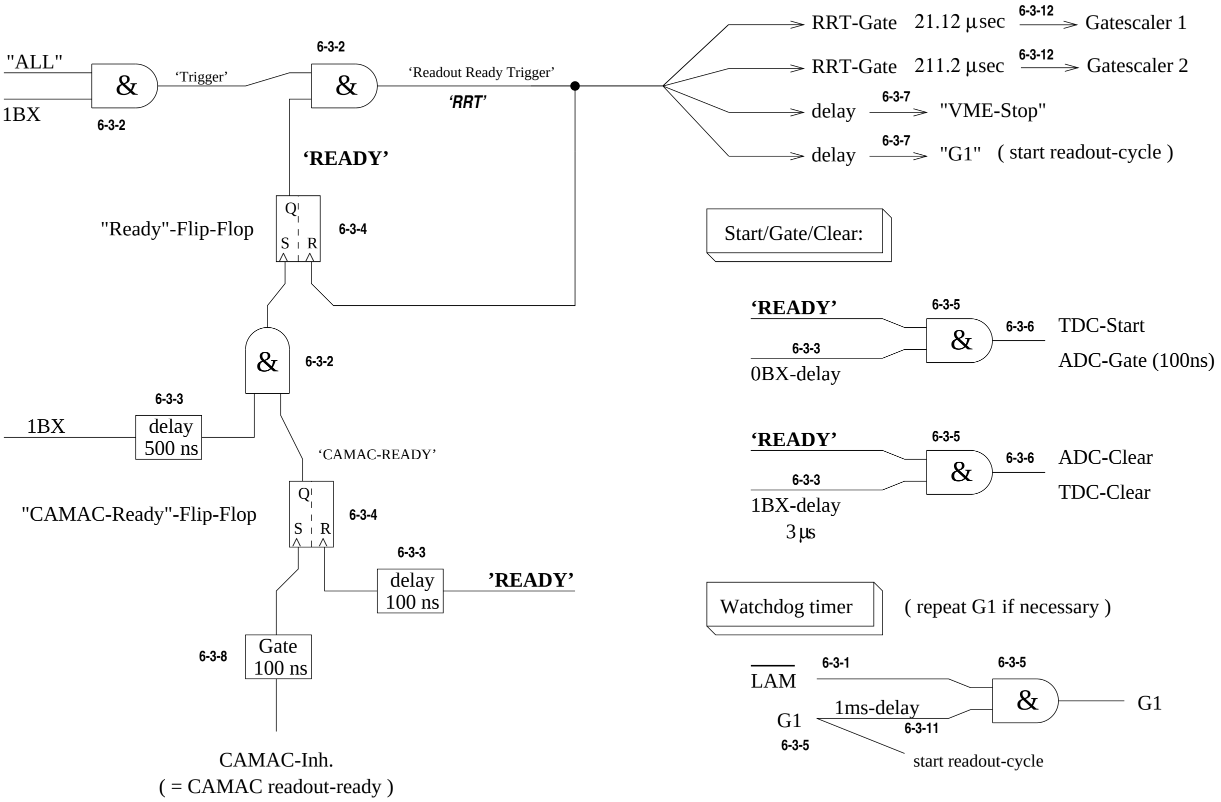


Figure 2: *Triggerscheme of the ‘Event’–Trigger 1998. The numbers show the slot of the accordant modules in the NIM–Crate.*

The processing of the different pulses and its temporal evaluation, as one can see in figure 3, is described in the following:
The HERA–bunchclock supplies a signal every first bunchcrossing (1BX–signal)[1]. If any coincidence of a triggercounterpair has appeared during this first bunchcrossing of 96 ns, a ‘Trigger’–signal will be generated. The ‘Trigger’–signal will only give rise to a data readout, if the “READY”–Flip–Flop is set to 1. As will be explained below, its output is set to 1, if the circuit is ready to perform a new readout cycle. The ‘Readout Ready Trigger’–signal (RRT) is then splitted into 5 pulses:

- RRT–Gate 21.12 μsec for gated scaler 1.
- RRT–Gate 211.2 μsec for gated scaler 2.
  These scalers count the numbers of defined signals during 1 (scaler 1) and 10 (scaler 2)

[1]The functionality of this clock will be explained in section 3

HERA revolutions.

- VME–stop; this signal will stop the digitalization by the FADC's. The delay will be adjusted in a way that a whole HERA revolution will be digitalized by the FADC's. The sampling frequency of the FADC's is derived from the BX–Signal that appears every 96 nsec and amounts 24 nsec.

- G1–signal; this signal starts the readout–cycle and has to be repeated if necessary (see section 1.4.

- Reset signal for the "READY"–Flip–Flop;

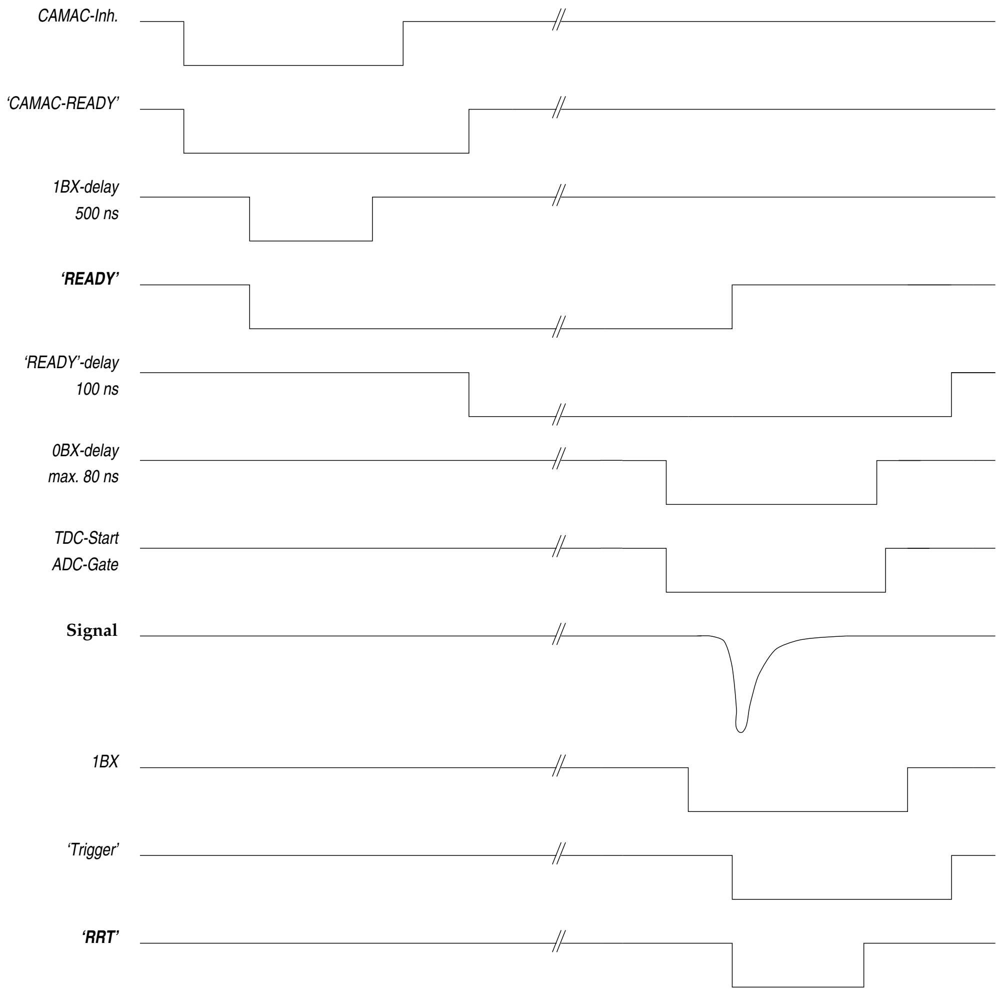


Figure 3: *Timescheme.*

1.2 'READY'–signal

The main elements for generating the 'READY'–signal are

1. the "Ready"–Flip–Flop that indicates that the circuit is ready to accept a trigger and
2. the "CAMAC–Ready"–Flip–Flop that indicates the completion of the computer's data readout cycle.

When the data readout cycle is finished, a 'CAMAC–Inhibit'–pulse is generated. This pulse is of no defined length and can be very long (in the range of ms to s). In order to avoid that the 'READY'–signal appears in this period and as a consequence both inputs of the CAMAC–"Ready"–Flip–Flop are set, the following was done:
From the rising edge of the 'CAMAC–Inh.'–pulse a pulse of 100ns width is created so that the possibility of synchroneous pulses at both Flip–Flop inputs is excluded.
To ensure that the output of the "READY"–Flip–Flop is set at a defined time, the 1BX–signal is delayed by 500ns and forms together with the "CAMAC–READY"–Flip–Flop–signal the *time defined* 'READY'–signal.

1.3 Start/Gate/Clear of ADC's and TDC's

The 'READY'–signal in coincidence with the 0BX–signal (a signal 96ns before 1BX–signal extracted from the HERA–bunchclock) forms a TDC–startpulse and an ADC–Gate. The 0BX–signal has to be delayed to guarantee that the signals of the photomultipliers coincide with the gate of 100ns.
The 'READY'–signal and the 1BX of 3 μs width in coincidence form a TDC– and ADC–Clearpulse if no interaction has taken place at the first bunch.

1.4 Watchdog timer

Because of the readout[2] computer's interrupt handling, it may happen from time to time, that the 'CAMAC–Inh.'–pulse is generated a significant time before the readout routine is left. This may lead to an interrupt of the whole data aquisition, because the G1–pulse for starting the readout is generated while the computer is stuck in the routine. To avoid this, we have to repeat the G1–pulse until the readout routine is left. This is task of the watchdog timer.

2 The 'Source'–Trigger

In order to calibrate the ADC's it should be possible to take data for pulses that will come from a radioactive source or a puls–generator. Therefore the trigger has to be modified to start the readout at any time a pulse is generated. For the setup of a sonamed 'Source'–Trigger the main goal was to start the readout–cycle if there's a particle from a radioactive source that crosses two szintillators behind each other at the same time. As it's described below, with a simple modification of the trigger setup it is possible to get this kind of trigger. The modifications are shown in figure 4 and described in the following:
First of all a "Coinc"–pulse must be generated from two scintillators behind each other. With this pulse the ADC–Gate is performed. The analogpulses of the two scintillators have to be delayed so that these pulses coincide with the ADC–Gate temporally.
The readout–cycle is started from the delayed "Coinc"–pulse, too. Except to this changes everything is equal to the 'Event'–Trigger described in section 1. The following section will show, how to get the so called "Coinc"–signal and how to modify the electronic.

2.1 Production of the "Coinc"–signal and modification of the electronic

The description below will help rebuilding the 'Event'–Trigger to the 'Source'–Trigger.

1. Give the two analog pulses to the first coincidence unit in slot number 9 (see figure 1). This will generate the "Coinc"–pulse;

[2] The whole digital information is collected in a VME–system. The data are send to a Linux workstation via ethernet and will be stored on a harddisk

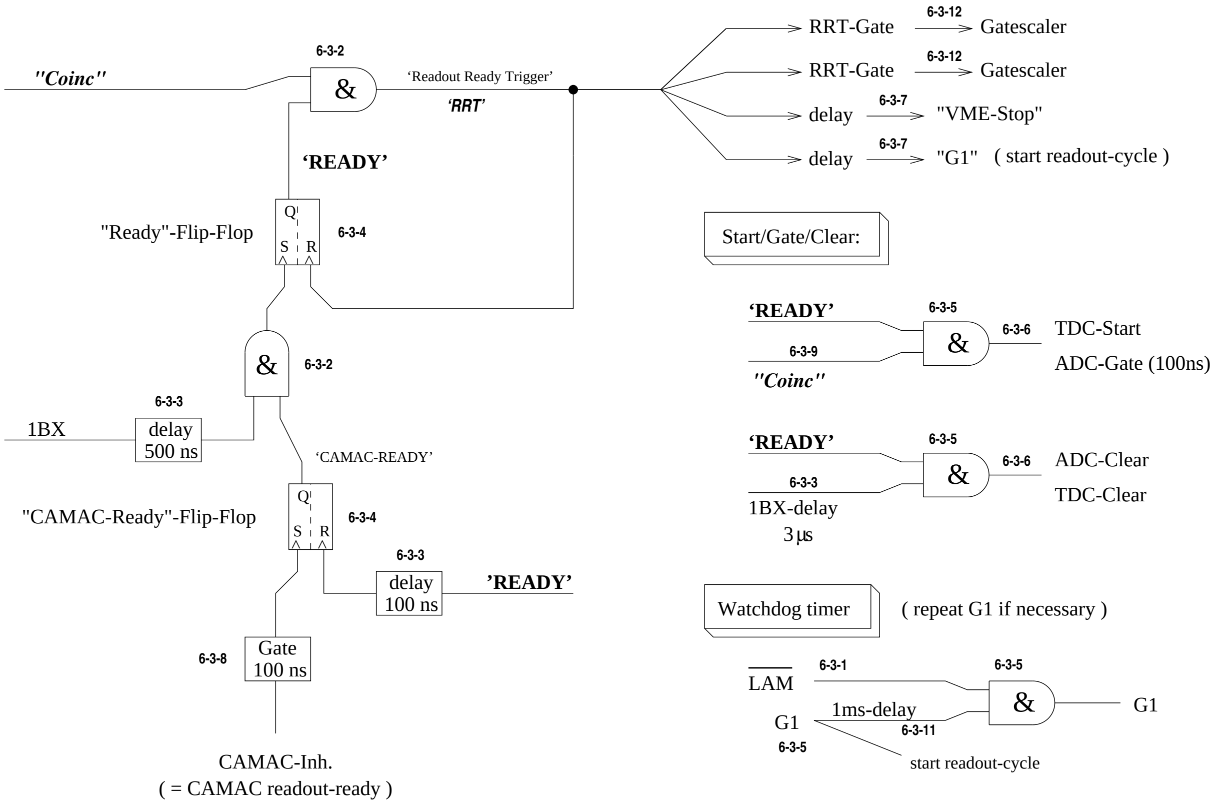


Figure 4: *'Source'–Trigger.*

2. Disable input B of the coincidence unit beneath and enable input A. This will make sure that the ADC–Gate is performed by the generated pulse;
3. Disable inputs A&B of the first coincidence unit in slot number 2 and enable input C. Then together with the 'READY'–signal the "Coinc"–signal will generate the 'RRT';
4. After a delay of 25–50ns through the delay box, the analog signals can be led into the input of the ADC unit that is gated.

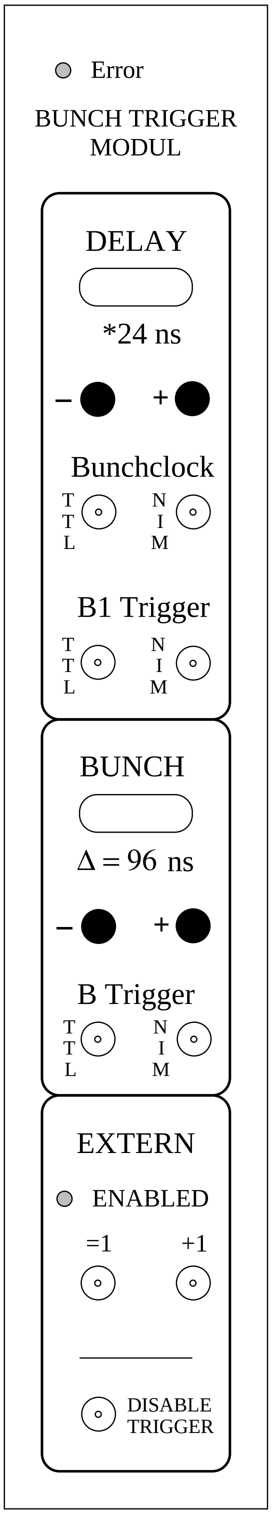
3 The HERA Bunchclock for protons

The HERA Bunchclock (HITp) is a very exact bunchclock and supplies signals that are correlated to the different bunches of the HERA protonbeam.
The so called BUNCH TRIGGER MODUL is shown in figure 5. The different functions of this module, the meaning of the signals and where they can be tapped[3] is listed below:

- Bunchclock: A signal for every bunch each 96 ns.
- B1 Trigger: A signal for a special bunch each $220 \cdot 96\,\mathrm{ns} = 21.12\,\mu\mathrm{s}$. If the DELAY is equal 0 a pulse is generated at the time the first bunch crosses the location of the wiretargets down in the westhall (this should be the setup, **sometimes different** !). This pulse can be shifted in steps of 24 ns with the black buttons below the DELAY display. For example in the case of a $48 \cdot 24\,\mathrm{ns}$ delay one gets a signal every time the 12th bunch is crossing the location of the targets.

[3] Each signal is supplied in NIM and TTL standard

- B Trigger: A delayed signal of x · 96 ns with regard to the adjusted B1 Trigger signal. x can be adjusted with the two black buttons below the BUNCH display.



Default values:

DELAY = 20
BUNCH = 219

Figure 5: *The Bunch Trigger Modul of the HERA Bunchclock for protons (HITp). The function and meaning of the different outputs are explained in the text.*