Hera-B 98-067
Outer Tracker 98-016

# HSPICE Simulation of the GTL input circuit of the HERA-B TDC chip

M. Beck
*University of Rostock*

**Abstract**

*As input circuit of the HERA-B TDC a Gunning Transistor Logic (GTL) circuit is used. This is the interface from differential signal of the ASD8 to the TTL logic inside the TDC. The behavior of the GTL circuit is simulated using the HSPICE package.*
*A nominal ASD8 signal with a pulse width of 15 ns, a swing of 100 mV at a base level of 1.25 V is reasonable to trigger the TDC.*

# 1 Introduction

The HERA-B TDC chip is build to measure the drift times (Time mode) inside the HERA-B Outer Tracker drift chambers. It is also possible to run this chip as a hit register (Hit mode) with 64 channels. This is done for the MUON,RICH and HPT sub detectors.
The chip includes eight time measuring circuits with a pipeline a FIFO and a test interface. Almost all signals are provided as TTL signals to the chip. Also the output signals are at TTL level.
To allow a suppression of external noise the detectors signals are provided as differential signals. The common used amplifier at HERA-B which supplies this differential signals is the ASD8. All differential signals have to be converted to TTL logic for the TDC chip. In Time mode the chip has eight differential receivers inside to do the signal conversion. The receivers are special GTL receivers by the company NEC. Running in Hit mode the TDC chip does not include all 64 receivers and a additional GTL-TTL converter is needed.
The GTL input circuit is simulated using the HSPICE package. The results presented in the following chapters are useful to define the working region and border conditions for the ASD8 signals.

# 2 The HSPICE model

The HSPICE simulation based on a model designed by the company NEC. It emulates the input GTL circuit for the TDC chip. The output is properly terminated as used inside the TDC chip and it supplies a low power TTL signal.
There are two input lines, the normal input V(in) and the inverted reference signal V(ref). Both signals are separate changeable. The interesting signal characteristic are the pulse length, the pulse width, the slope of rising edge and the base level. The pulse width is the time between the 0.5 value of the rising and falling edge of the signals. As pulse high of swing the amplitude from low to high level of a signal is meant. The base level is the constant voltage around which the input signals swing and it is set on the TDC board. A slope, rise or fall time of a signal is the time between switching from low to high level or vice versa. All this parameters are independently adjustable inside the simulation for both input lines. The simulation time is sampled in steps of 0.1 ns over a range of 100 ns.

# 3 The Simulation

The following simulations are done to find out the border conditions, which kind of ASD8 pulses trigger the TDC and what is the optimum working point for the GTL receiver. Results from the simulation are shown in the following sections grouped by the parameter which were changed.

## 3.1 The slope of rising edge

A important parameter is the rising slope of the ASD8 signal. This rising slope triggers the time measurement in the TDC. To find out the influence of different rise times of the ASD8 signal on the time measurement simulations with different slopes were made. Here

both input signals are assumed to be symmetric* around a base level of 1.25 V and have a pulse high of 100 mV. The GTL rise time is changed in steps of 0.5 ns in the range from 0.5 to 10 ns. The measured transition time is the time between the 50% values of the input and output signal.
The simulation is done for 3 temperatures. Normal temperature of 25° C is the assumed temperature with cooling in the west hall. High temperature of 50° C is the mean temperature without cooling and -70° C is a reference temperature.
A typical signal with a rise time of 3 ns is shown in figure 1. The transition time here is 1.68 ns for a temperature of 50° C. Figure 2a displays the 50% time, for the TTL output

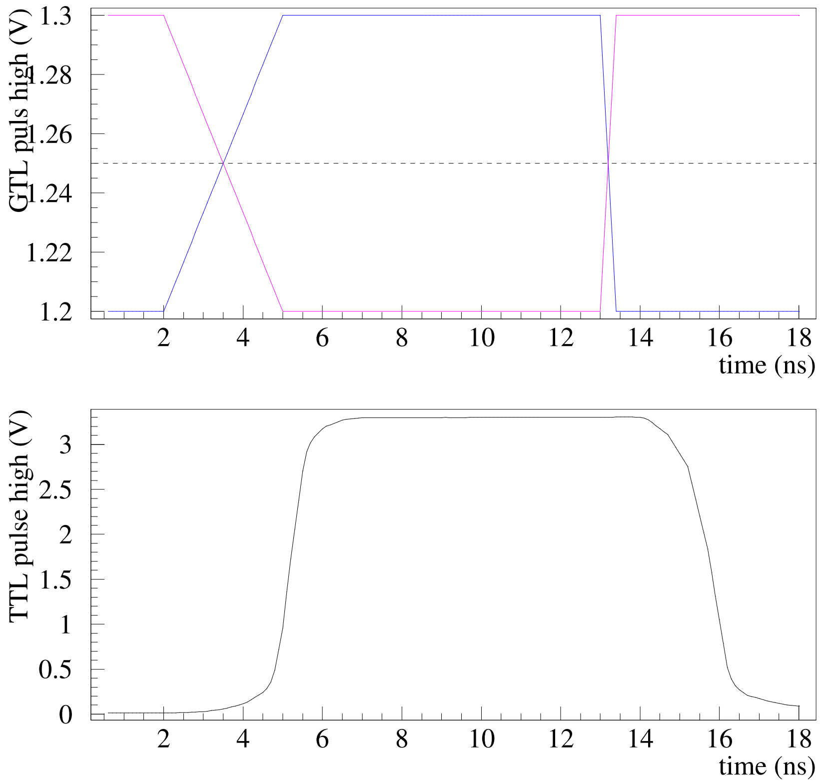


Figure 1: Example for a GTL signal with a rise time of 3 ns. The corresponding TTL output signal has a transition time of 1.68 ns at 50° C

signal versus the 50% time of the GTL input signal. It shows a proportional behavior of the two signals inside this range. A more detailed view into allows the transition time which is the difference of the previous time values. The resulting plot of the transition time versus GTL rise time is shown in figure 2b. Two effects are visible. The first thing is a maximum transition time at a rise time of about 5 ns. This leads to a maximal time uncertainty for the drift time measurement of about 0.3 ns due to fluctuations on the rising slope of the ASD8 signal. A reasonable drift velocity of 13 cm/$\mu$ leads to a uncertainty of about 40 $\mu$m. This is a minor effect for the OTr resolution.
The second point is the temperature dependence of the transition time. A temperature drop of 25 degrees from 25° C to 50° C leads to an error of 0.1 ns.
Both uncertainties give only a small contribution and are neglect able for the final OTr resolution ($\mathcal{O}$ 200 $\mu$m). An effect which is not considered is the smearing due to uncertainties at the 50% trigger threshold. This effect is clearly larger for larger rise times. A solution is to have rise times less then 4 ns at the ASD8 signal.

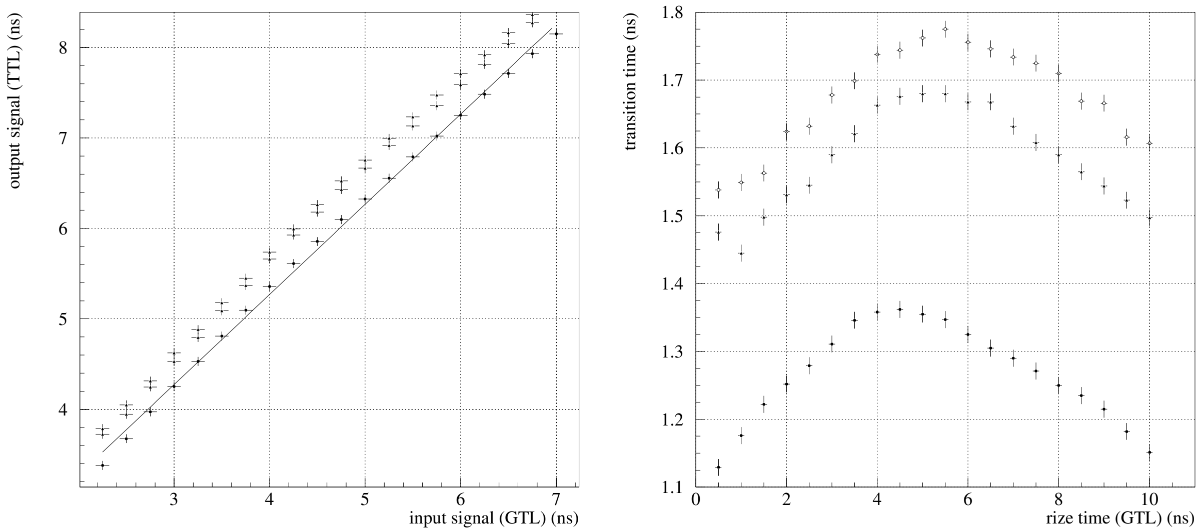


Figure 2: The pulse length of the GTL input pulse versus the TTL output pulse length is drawn. The transition time is the time difference between input and output signal. It is plotted versus the rise time of the leading edge. The plots include data from temperature 25° C, 50° C and -70° C.

## 3.2 GTL pulse width

A simulation of the GTL input circuit with different input pulse width should give the minimum width which is able to trigger the TDC. This information is necessary to exclude noise triggering of the TDC due to small spikes. To get only the influence of the pulse width the other parameters are fixed. The values are 1.25 V base level, 100 mV swing and a rise time of 0.1 ns. The pulse width was varied in a range from 0 to 25 ns with a step size of 1 ns and 2 ns.

A typical plot with a GTL pulse width of 10 ns and the corresponding TTL signal is shown in figure 3a). The rise time of the input signal is choosen as 0.1 ns to have no influence in the pulse length studies. The GTL circuit reacts with a low power TTL signal, rise time 0.5 ns, low level 0 V and high level 3.3 V.

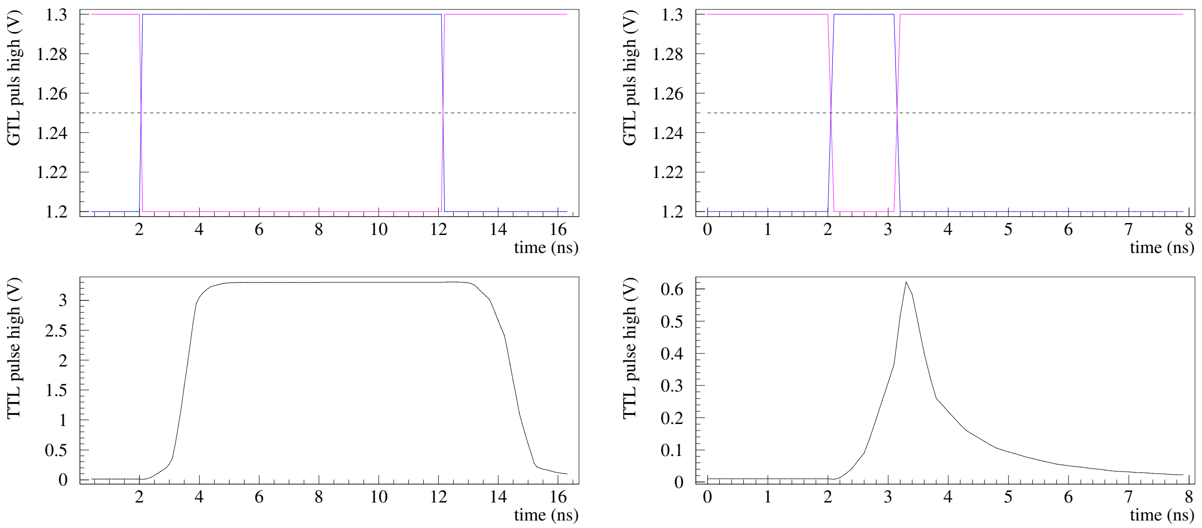


Figure 3: Example for a GTL signal with a rise time of 0.1 ns and a length of a) 10 ns and b) 1 ns. In a) the corresponding TTL output signal has a rise time of 0.5 ns and a standard (high=3.3 V low=0 V) shape. Case b) shows an output signal which is not a TTL signal.

Varying the GTL pulse length a limitation due to the input pulse length is found at 6 ns. This dependence is characterized by a the GTL output signal high and length. Both values, the pulse high and the difference of input and output pulse length are plotted in figure 4b). Figure 4a) shows that the pulse length at the input and at the output of the GTL circuit are in linear dependence.

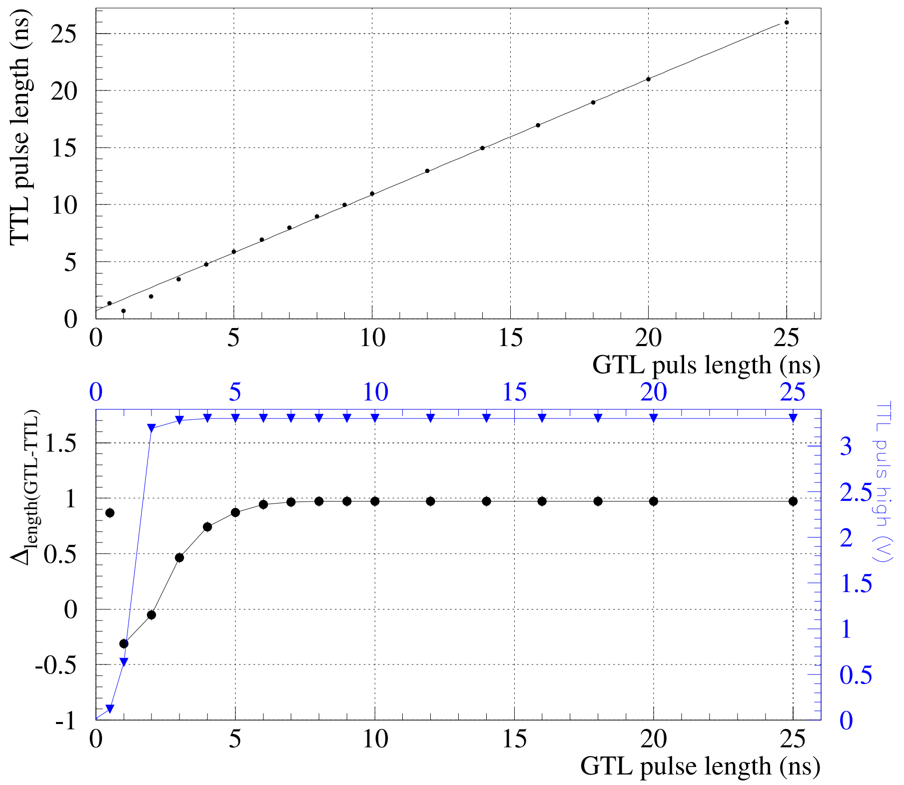


Figure 4: a) The pulse length of the GTL input versus output signals is linear above a minimum pulse length. b) Pulse high and difference of pulse length give the minimum trigger values of 3 ns and 6 ns.

One can summarize the trigger behavior of the GTL receiver as follows. At a minimum pulse length of 3 ns the receiver starts producing an TTL-like output signal. But the output signal length becomes linear with input length above 6 ns. We assume that the TDC is only triggered with a stable TTL signal. The simulated lower limitation in pulse length for triggering the GTL and the TDC is found at 6 ns.

## 3.3 GTL pulse high

The high of the input pulses is like their width a criteria which allows to decide at what kind of noise or chamber signals triggers the TDC.
The amplitude from low to high of an input signal is the pulse high or the swing of the signal.
In the following simulation the both input signals are assumed to be symmetric around a base level of 1.25 V. Signal slopes are set to 0.1 ns to have no influence on the simulation. The pulse high is varied in steps of 10 mV in a range of 10 to 200 mV. The pulse length is

fixed to 10 ns which is 10% of the bunch crossing time at HERA-B.
Figure 5 shows two input signals with there corresponding output of the GTL chip. In case a) a input signal with 100 mV swing produces a nominal TTL output. The second example has a swing of 10 mV. Here one can see that the GTL circuit output has from TTL different high and low levels.

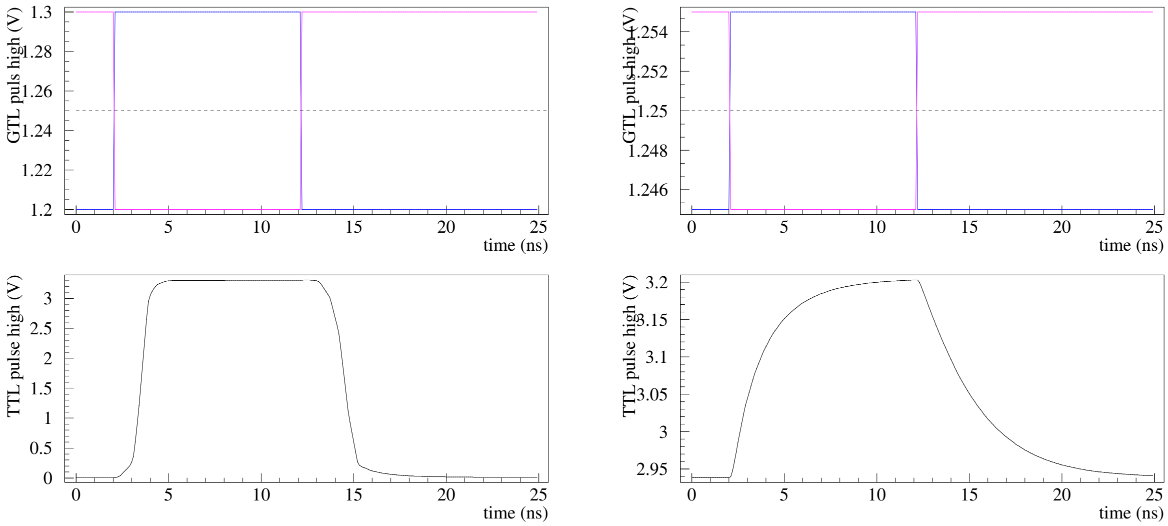


Figure 5: A GTL signal with a rise time of 0.1 ns a length of 10 ns, and a swing of a) 100 mV and b) 10 mV. In a) has the corresponding TTL output signal a rise time of 0.5 ns and a standard (high=3.3 V low=0 V) shape. Case b) shows an output signal which is not a TTL signal.

The criteria to find the minimum pulse high is the point at which the GTL output reaches normal TTL shape (low=0 V and high 3.3 V).
In figure 6 are the TTL output level values for the different GTL pulse high drawn. The second plot shows the difference between the high and the low level of the TTL pulse.

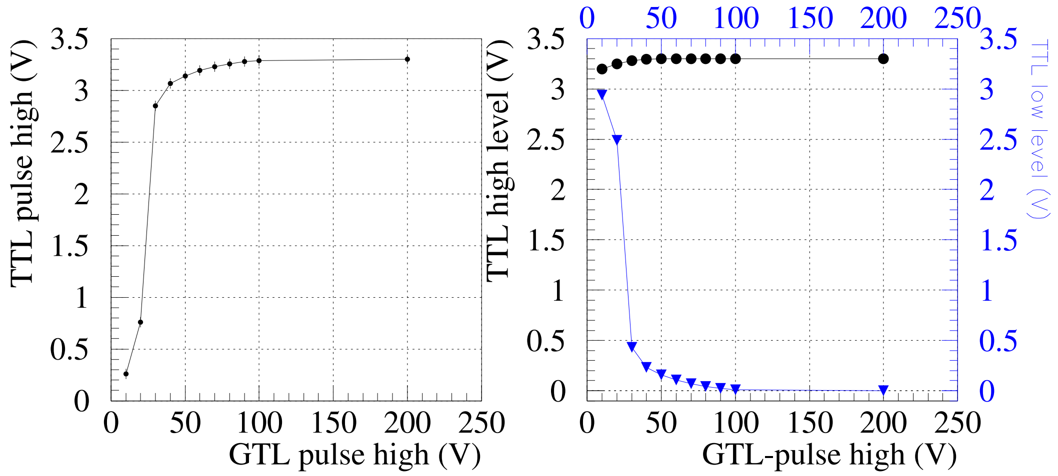


Figure 6: Pulse high of the TTL (output) signal versus pulse high of GTL (input) signal is constant above 100 mV. The corresponding high and low levels for the TTL pulses are drawn in the right figure.

At a swing of 40 mV the GTL receiver starts to be efficient. A stable level with constant output signal is reached at 100 mV which is the by the company proposed value.

## 3.4 GTL pulse base level

The fourth parameter in the GTL pulse is the base level. This is a constant voltage around which the GTL (ASD8) signal switches.
To find the minimum and the maximum usable value, the base level is varied in steps of 25 mV from -1.5 V to 3 V. The two input signals are symmetric with a swing of 100 mV, a slope of 0.1 ns and a pulse length of 10 ns.
In figure 7 are the GTL signals with their TTL outputs shown for base levels of 1.5 V and -1 V. One can clearly see that at -1 V the output signal does not reach the low (0 V) and high (3.3 V) level.

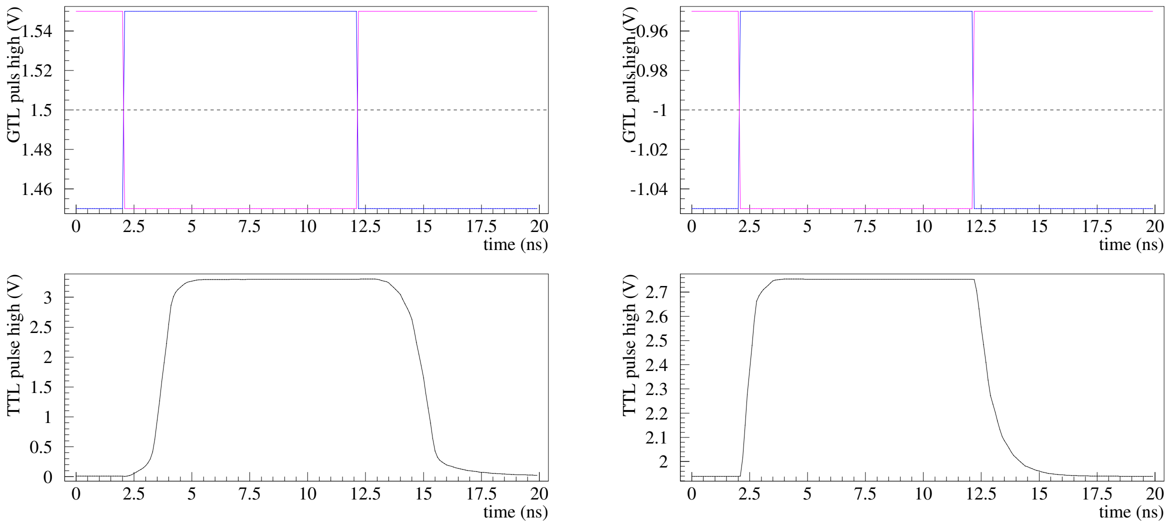


Figure 7: Example for a GTL signal with a rise time of 0.1 ns and a length of 10 ns, a) base level of 1.5 V or b) base level of -1 V. In a) the corresponding TTL output signal has a rise time of 0.5 ns and a standard (high=3.3 V low=0 V) shape. Case b) shows an output signal which is not a TTL signal.

The characteristic values for the output pulses are plotted in figure 8 for different base levels. A dynamic range of about 2. V is found between -0.5 V and 2.1 V. Below this range the output signals doesn't reach the nominal levels and also the pulse high decreases. At 2.1 V the high level goes to zero and above 2.2 V both levels are at permanent high (3.3 V).

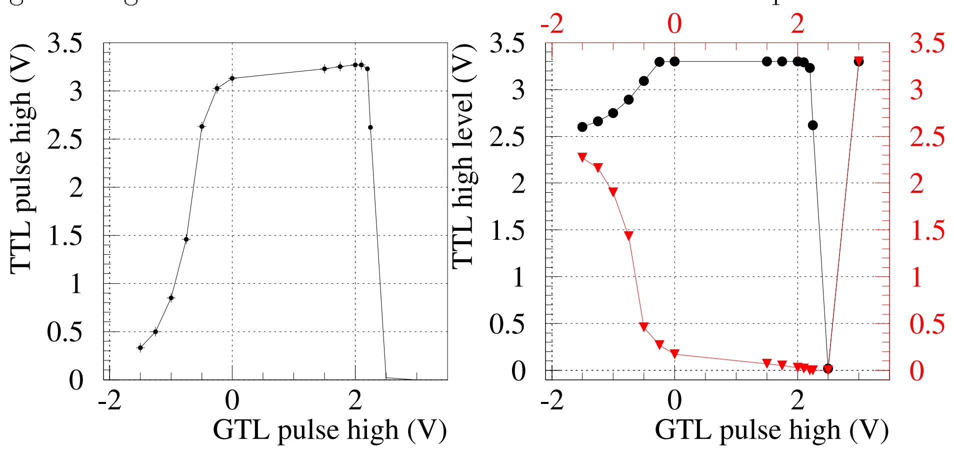


Figure 8: Variation of the GTL base level. Left: Pulse high versus base level and right: low and high levels of the TTL (output) pulse versus base level.

The standard value of 1.25 V is in the middle of the dynamic range. All TDC boards are adjusted to this nominal voltage and this was also tested with over 3000 ASD8-TDC channels.

### 3.5 GTL input asymmetry

The differential signals are driven from the ASD8 via twisted pair cable to the TDC. It can happen that due to broken cable, bad connection (resistance) or different cable length the two inputs receive asymmetric input signals. This section should clarify the influence of the asymmetry and the minimum overlap of the two input signals.

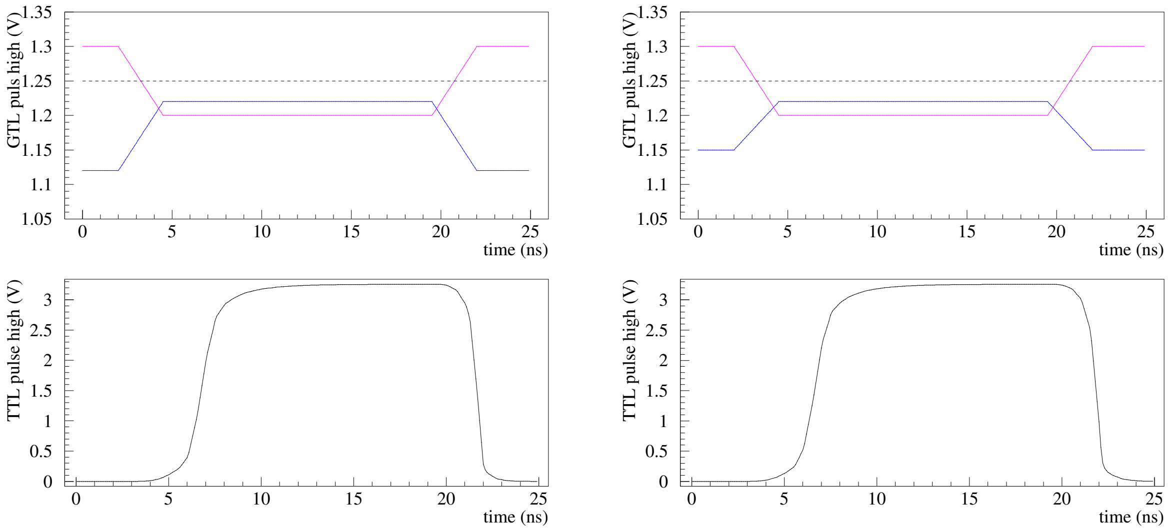


Figure 9: Examples for GTL signals with 10 mV overlap, a rise time of 3 ns and a length of 15/,ns and reference Signal at 1.25 V with 100 mV a) V(in) with 100 mV swing and a shift in base level. b) V(in) with constant low level and 70 mV swing. The corresponding TTL output signals are equal.

Therefore two simulations were done. The fixed values for both simulation are the swing and offset of the reference input V(ref) at 100 mV and 1.25 V, the pulse length with 15 ns and the slopes with 3 ns.
In the first study the base level of the input V(in) was varied and the pulse high was constant. For the second analysis a variable pulse high at constant low level was used. Figure 9 shows examples for both methods at the same overlap of 10 mV of the input signals.
Both simulation methods give the same result which is presented in figure 10. Here you see the calculated amplitude of the TTL level and the TTL high and low level found for each simulated point. The minimum overlap were the GTL produces reasonable TTL pulses is found at -10 mV. A negative overlap means, if the input pulses V(ref) and V(in) come closer than 10 mV a output signal is produced, the TDC is triggered.
Real chamber pulses should overlap more than 50 mV which is the begin of the stable range.

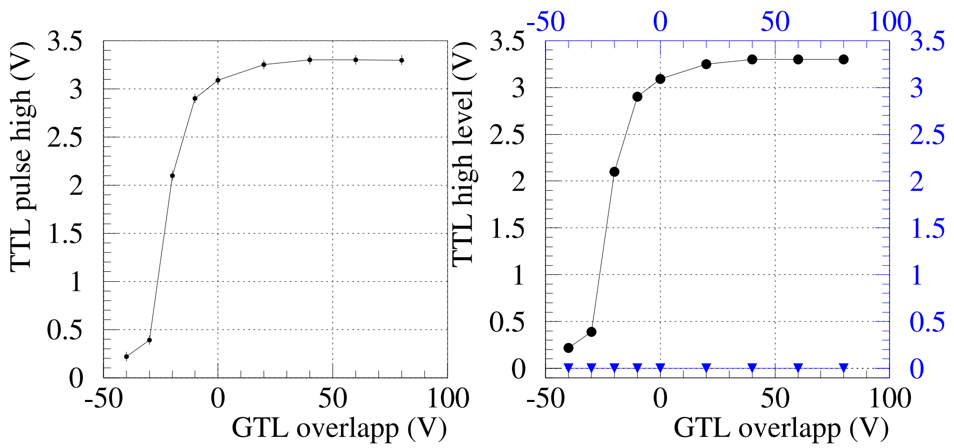


Figure 10: Variation of the overlap of the GTL input signals. Figure a) shows the calculated amplitude of the TTL signal and b) shows the high and low level of the TTL pulse. The lower limit is found as

### 3.6 Conclusion and demand

Most of the simulation results as pulse high, length and base level shift were also furnished in in several experimental setups. Therefore the TDC chip was extensively tested at the HP-tester (see [1]) and also in different other setups using modified ASD8 signals([2]).
Summarizing all simulation results together one can define a standard GTL signal provided by the ASD8. This nominal signal is displayed in figure 11a). It has a rise time of 2.5 ns a length of 15 ns and it is symmetric with a swing and overlap of 100 mV. This is what we demand for the TDC to be away from the critical limits.
A possible range for the input signals is sketched in figure 12. The base level should lie between 0 and 2 V the swing around 100 mV, but not below 50 mV and a pulse length is demand to be larger then 6 ns.
In our experimental setups are ASD8's used which supplies signals with >100 mV swing (at a Voltage of ±2.5 V) (see [3])

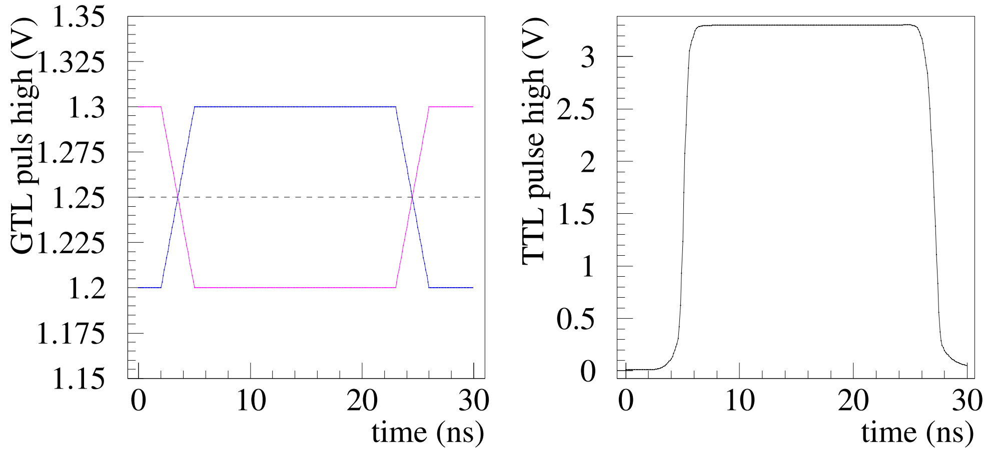


Figure 11: A nominal GTL (ASD8) pulse simulated with HSPICE (rise time 2.5 ns, length 15 ns, swing 100 mV).

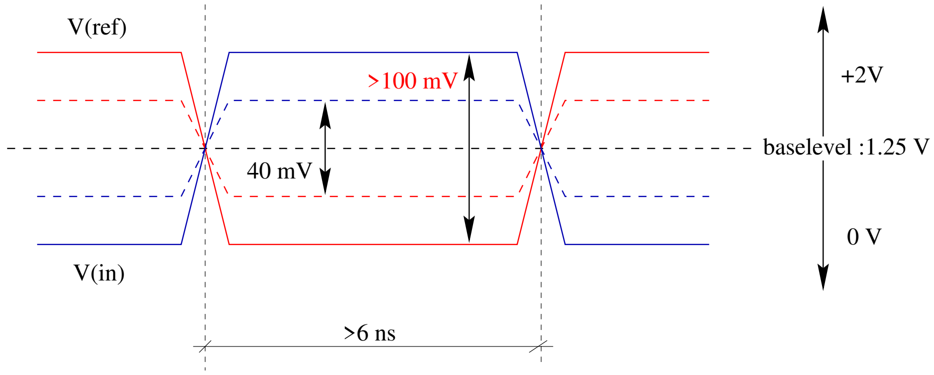


Figure 12: Schematic overview of the limits for the GTL (ASD8) signals. restrictions given by the GTL receiver integrated in the TDC chip.

# References

[1] M. Beck, R. Zimmermann
*Methods and Results of the TDC-Hit-Chip Test at Heidelberg*
*DESY Hamburg , June 1996*

[2] M. Beck
*Studies of base level influence to ASD8 output signal*
*Talk at the OTr meeting*
*IFH Zeuthen, March 1997*

[3] M. Beck, R. Zimmermann
*Working point measurements of Honeycomb Drift Chambers*
*DESY Hamburg, March 1998*