Hera-B 96-192
DAQ 96-012

Method's and Results of the TDC-Hit-Chip Tests at Heidelberg

R. Wurth (DESY)
M. Beck, R. Zimmermann (University of Rostock)
June 05, 1996

1 Introduction

This note gives a short overview about the results of the TDC-chip tests with the HP-chip tester at Heidelberg. The method's to test the features of single components are described in detail. In the first part there will be a description of TDC in-chip units. Then you will find a explanation of the used methods with the HP-chip tester. Finally there will be a summary of the test results.

2 The TDC-Chip

2.1 The place of the TDC chip in the readout electronic

The TDC-chip is only one important part of the whole readout electronic (Fig. 1). Here electronics are necessary to process the pulses from the detector components. For this the TDC chip converts signals into digitized times or it acts as a Hit register. The readout electronics consists of the ASD8 board, which acts as the preamplifier and amplifier, the SHARC board as second level buffer (SLB), the fast control system (FCS) to control the several components and coordinate the control signals and finally the VME controller to readout the SHARCs and store the data. Then you may access the data from the memory (disc) to make analysis.

2.2 Superstructure of the chip

Figure 2 shows the layout of the TDC-chip developed by DESY. The TDC-chip is a CMOS-chip within a 160 pin-package of 0.6 μ technology. The TDC is an Application Specific Integrated Circuit (ASIC) designed by the company MSC and produced by

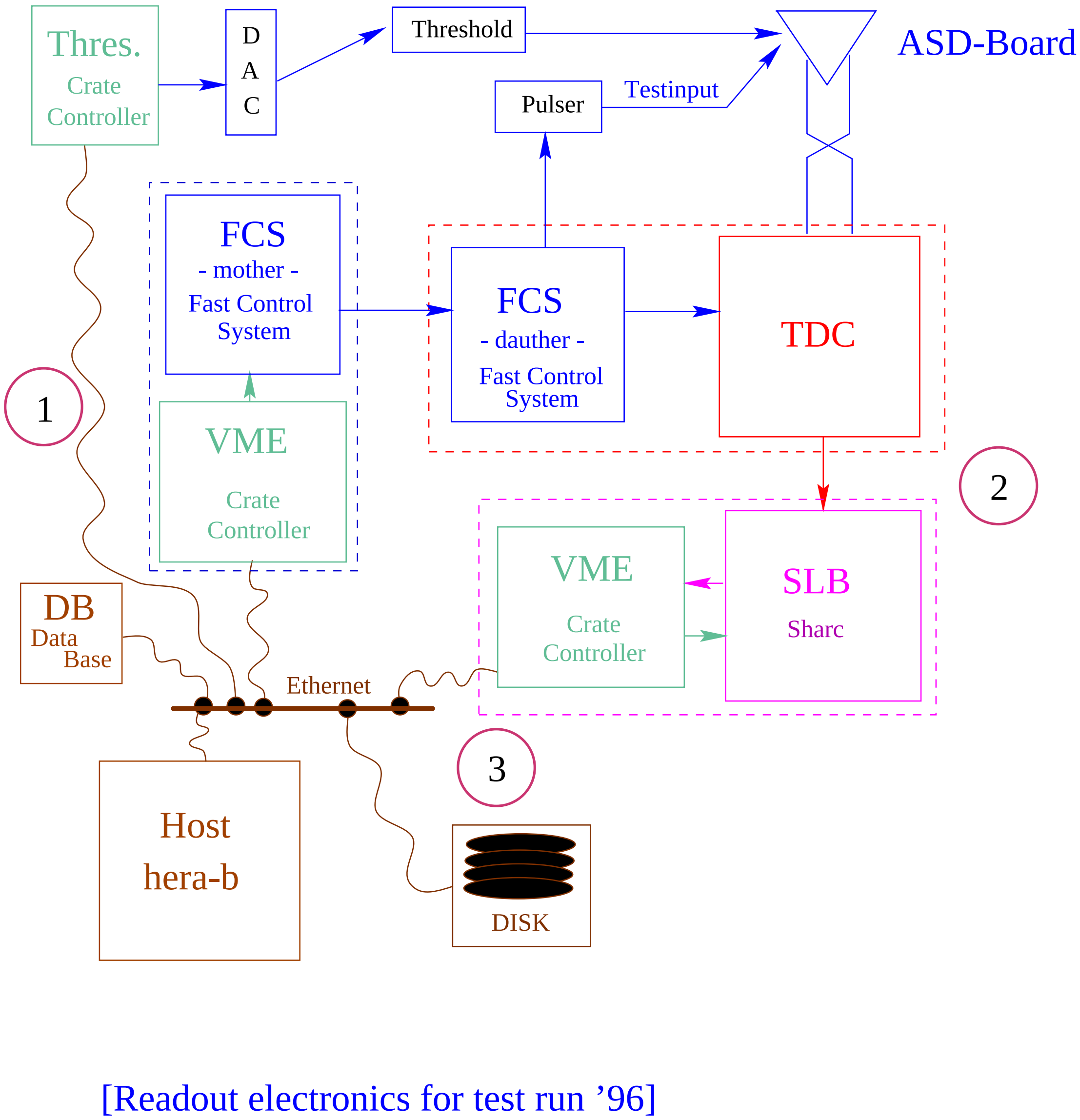

Figure 1: Place of the TDC chip in the readout electronic

NEC. The TDC-chip includes the following features (Fig. 2):
– 8 GTL inputs for the differential ASD-Pulse
– Test device - a test generator for all input signals
– Hit output register (with optional OR) for the **F**irst **L**evel **T**rigger
– 8 x 8 Bit **T**ime to **D**igital **C**onverter
– Buffer memory PIPELINE (ring-buffer)
– Derandomizer FIFO memory
– Readout buffer with addressing unit
– Calibrating unit (with high speed multiplier)
– Chip select feature
– Hit input register for 64 channels

2.2.1 GTL inputs

The GTL inputs are special, designed by NEC. There are differential inputs which have a minimum swing of 50 mV and a maximum swing of 200 mV. The base-level is around 1.250 V [Fig. 3]. The ASD-8 board supplies a swing of normally 160 mV around a base-level of 0 V . Therefore we need a level-shift for the ASD8 output from 0 V to this base realized by two 62Ω resistors (each for one channel) to +1.3 V power. All other inputs and outputs of the TDC-Chip need TTL level.

2.2.2 Test unit

For testing the components of the TDC chip, a test device was used to generate several test pattern for pulsing the definite channels. The test device supplies three modi, the odd, the even and the all channel mode. It has a 3-bit input for setting the functions. Both the first bits (0 and 1) control the modi and bit two at PIN 19 starts the test measurements. Bit zero and one have to be configured as follows:

Table 1: Set the test pattern

Function	BIT 0	BIT 1
even	1	0
odd	0	1
all	1	1
off	0	0

If one switches the test device on, all other inputs like GTL inputs or Hit inputs are disabled. That is most useful for testing the chip without having disconnect it from the detector.

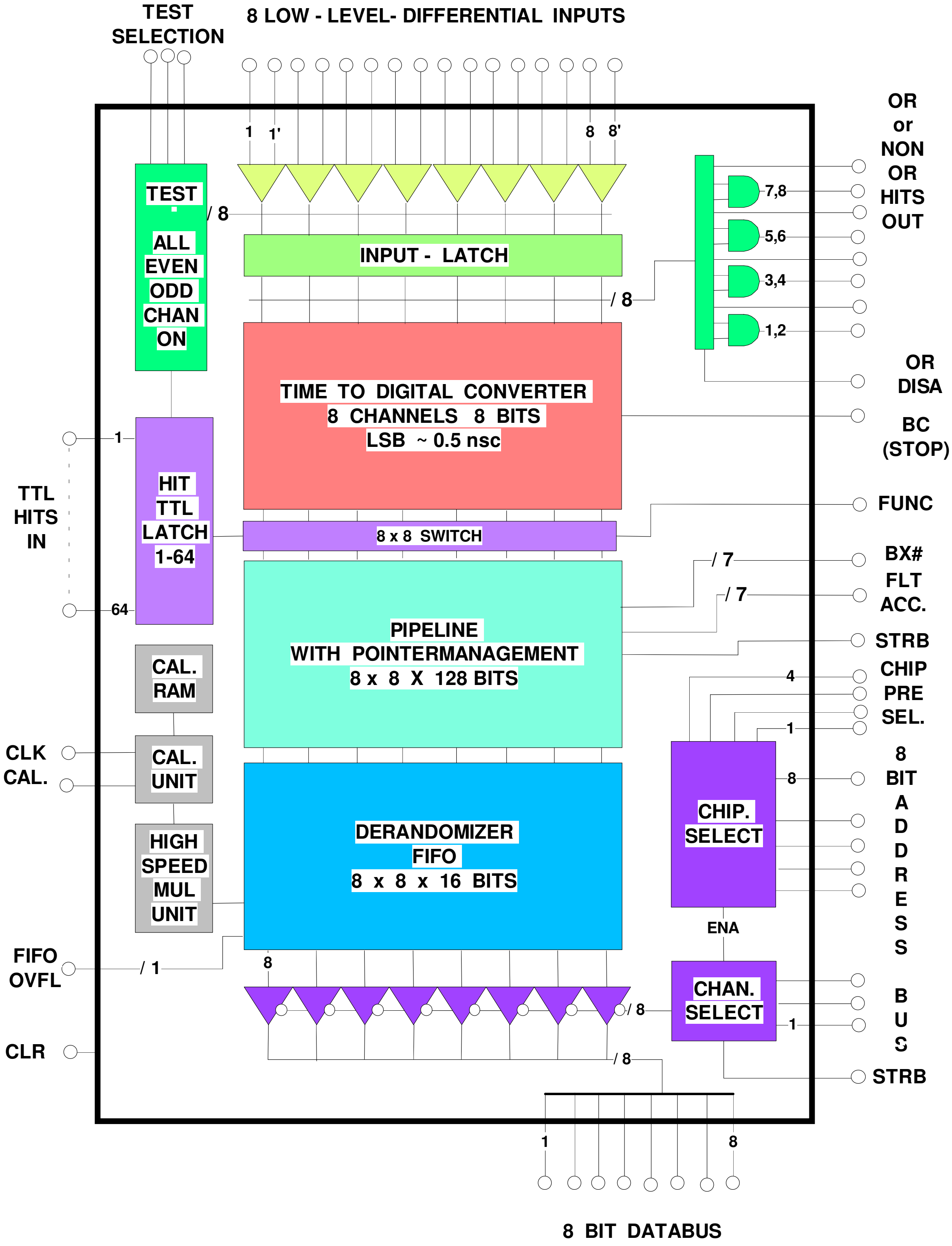

Figure 2: Layout of the TDC-chip

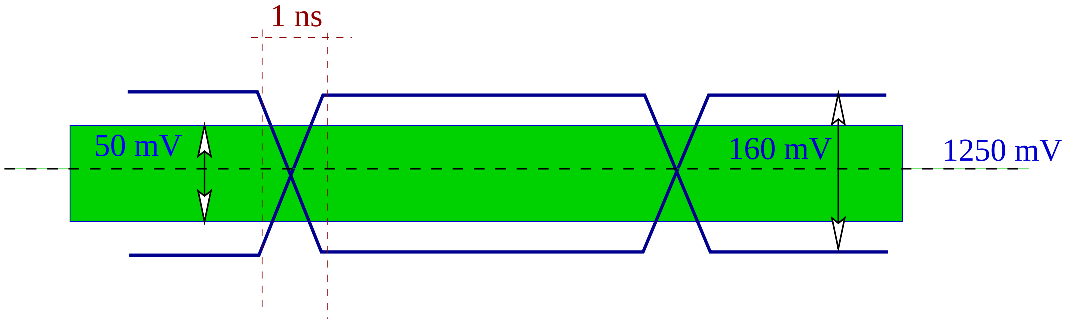

Figure 3: GTL level definition

2.2.3 The Hit outputs

The Hit output (Fig. 2) gives a signal for those channels which have been attached in the last bunch period. Normally the Hit outputs are ORed (logical) pairwise but this OR can be disabled optional by setting PIN 56 to high level (pull down in Chip). The Hit outputs will be used for the First Level Trigger (FLT).

2.2.4 The TDC circuit

The heart of the chip is an 8 bit TDC circuit. Such a circuit is needed to convert time differences into digitized times. There are 9 circuits, eight for time measurements and the 9^{th} is integrated for temperature calibration. Every 0.8 secs the 9^{th} channel measures a given time interval. Then a calibration factor will be calculated from the time difference of two measurements. So the time from each channel 1 up to 8 will be multiplied by this factor. This is done during the transfer from the derandomizer. So that the Chip may compensate for temperature and voltage variations.
The measurements are done in common stop mode. The START is given by the pulse from the GTL-Input or test device and the STOP is given by bunch crossing end. The results are written to a buffer memory (pipeline).

2.2.5 The Pipeline

The PIPELINE is a ring-buffer memory of 8 bits per cell and channel. Each ring-buffer consists of 128 cells. After 128 write cycles the first cell will be overwritten. The writing procedure is as follows: a BX-pointer is pointing at a cell with the BX number as address and the event would be written there. In the next bunch crossing period the BX-pointer points the next cell, and so on. The BX-pointer increments from 0 up to 127. So the First Level Trigger has a maximum time of 12 μs (96 ns * 128) for finding a good event. The 96 ns is the length of a bunch crossing period. If there is a good event, the Fast Control System (FCS) gives a FLT number which correspond to the

BX-pointer and the FLT-Accept pushes the event data to the FIFO.

2.2.6 The FIFO and the readout unit

The derandomizer FIFO is a buffer memory for each TDC channel with a depth of 16 events. Here the events are stored for the readout by the Second Level Buffer (SLB sharc). The readout is organized by the channel select unit which addresses every single channel buffer. The FIFO gets full if readout is to slow, the next event will be lost and the FIFO-overflow is set.
When the readout procedure is finished, the high speed multiplier unit (Fig. 2) updates the TDC values. This causes a delay of 500 ns between readout the last channel and readout the first channel of the next event.

2.2.7 The TDC chip as hit register

In addition this TDC-Chip can be used as a HIT register. That means, if one sets the Function Bit [PIN 24] HIGH (pull down in Chip) the Hit inputs 1 to 64 are enabled. The Hit inputs are put in groups of 8, so we get the same 8 bit data-format as the TDC. The managment between PIPELINE and FIFO is identical, regardless of weather the chip is acting as a TDC or HIT Register (read above). In this case the TDC circuits are disconnected. Only the test device is working like described above.

3 The test equipment

The equipment used is shown in Fig. 4. For the TDC chip test in Heidelberg a chip tester from Hewlett Packard (HP 82000) was used. It has the ability to define 48 pins as dynamic input or output. Furthermore four pins are used for power supply. The tester is controlled by a HP machine (APOLLO). This controlling is done by a specific software package. To work with the tester the timing, levels, pulse form etc have to be defined. The monitoring of the pin states was checked with a scope. The results are checked in terms of a multichannel analyzer (special program of the software package), to find out errors in the timing.

The adapter board (Fig. 5) was used to connect the chip and the HP-Chip tester, because only 48 pins (of 160) at each time were accessible. So its possible to select the TDC chip pins which are necessary for each function test. The adapter board consists of two boards, a gold adapter board for connecting the tester with the test board and the test board itself. The gold board serves as the distribution of the power and the ground to several pins of the test platine, as well as for the mechanical stabilization. The test board is a four layer platine with 124 pins. 48 hit I/O channels for controlling the dynamic functions of the chip and the rest is combined to power and ground. The

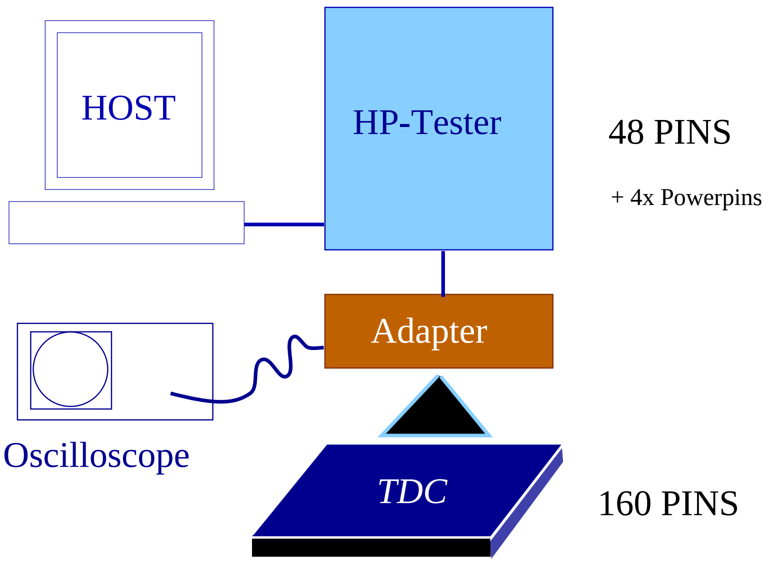

Figure 4: Scheme of the used test equipment consisted of the TDC chip, connected with the HP-tester by a special test board, of a scope and a HP computer as control platform

board has 16 switches to control the static functions for the Chip. In table 2 the possible dynamic pins are shown.

The static switches are specified in table 3. In addition there are pull up resistors on the test board to pull up the open states to a known level (+5V). The connectors on the board distribute the available pins. For example there are eight GTL inputs but only two are accessible at the same time, by connecting the particular two channels with the tester pins. The TTL Hit inputs are distributed in the same way (eight of 64).

4 The test of the TDC chip

4.1 General Hints

The minimum time period of the HP-Chip-tester was chosen as 25 ns. So the bunch clock will take 100 ns (50% High and 50% LOW). In this part the 10 MHz reference clock (Cal-clock) is equal to the bunch-clock. All input and output signals excluding the GTL-input are of TTL type. To get a lower power consumption the outputs have pseudo TLL, so the high level is 2.95 V (Fig. 6). After each power pull-up the chip has to be reset. This is done by the following (Fig. 7):
1. connect the BX-Clock, Calibration Clock;

Table 2: Pin functions of the test board

dynamic functions	number of pins	explanation
BX#	7	number of cell to write with the BX pointer
FLT#	7	number of cell to read out with the FLT pointer
FLT_ACC_STRB	1	start for read out the pipeline
DATA_OUT	8	data output from the TDC
ADDR_CHAN	3	channel select for data output
STRBDATA	1	start for read out the FIFO
CAL	1	input for calibrations clock
RESET	1	reset input
FIFOVFL	1	output for FIFO overflow
HITOUT	8	output for monitoring the GTL inputs (FLT)
BXCLK	1	input for bunch clock
TEST_STRB	1	start for measurements with test device
START	4	2 of 8 GTL inputs
HITIN	4	4 of 64 HIT inputs

Table 3: switches

switch number	switch	explanation
TEST0	1	bit 0 for test pattern
TEST1	2	bit 1 for test pattern
FUNC	3	change between GTL or HIT inputs
LORESO	4	bit to get half the resolution
PRESEL1	5	chip selection
PRESEL2	6	chip selection
PRESEL3	7	chip selection
PRESEL4	8	chip selection
ENAGTL	9	enable the GTL inputs
TESTIN	10	input for switch into the special mode
ADDR3	11	chip address
ADDR4	12	chip address
ADDR5	13	chip address
ADDR6	14	chip address
ADDR7	15	chip address
ORDISA	16	logical OR for HITOUTS

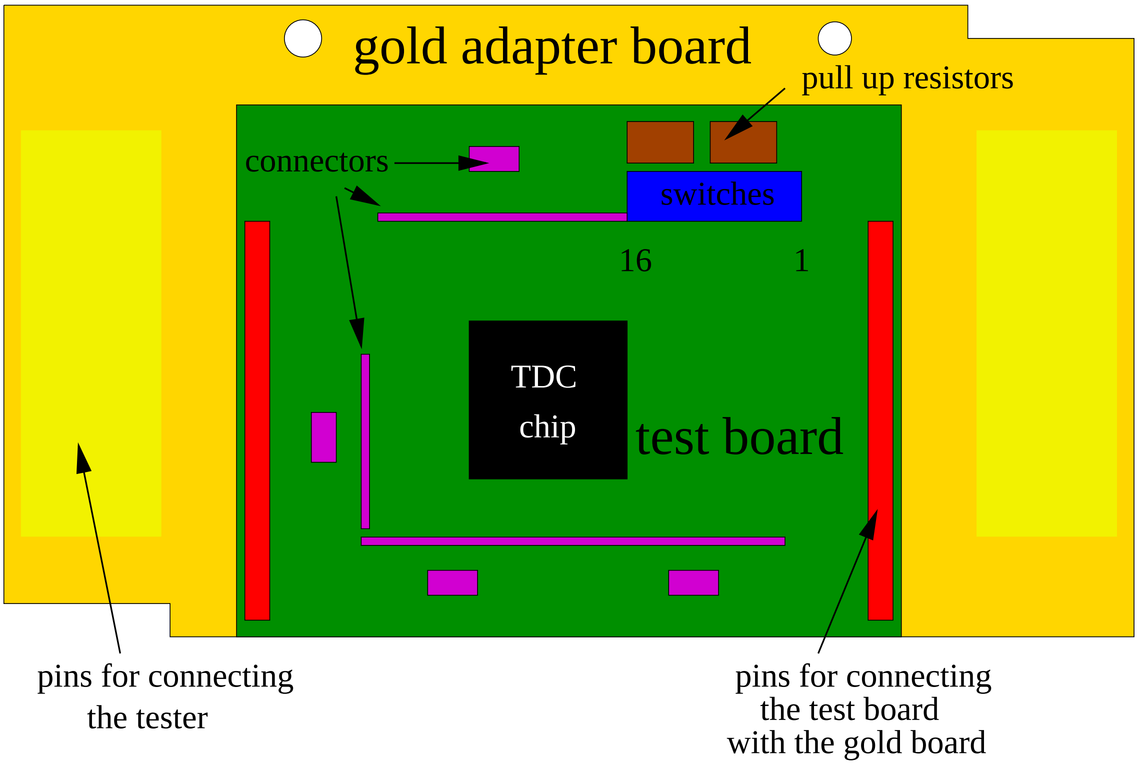

Figure 5: Schematic presentation of the adapter board and the test board

2. set the reset input (PIN 27) for $\approx$ 175 ns HIGH;
3. wait for $\approx$ 12 μs

4.2 Time measurements with Test-strobe

To test the TDC circuits, it's not necessary to disconnect the TDC chip from the readout electronics. If one sets a pattern at the test-device the GTL inputs are internaly disconnected. After connecting bunchclock, calibration clock, FLT- and BX-number the test-run is prepared. If the pattern is set (Tab. 1) the rising slope of the test-strobe (positive pulse inside a bunch) gives the start for time measurements. The stop comes from the falling slope of the bunch-crossing end. The input time is then the difference between start and stop (Fig. 8). The measured times were written into the pipeline at the cell where the BX-number is pointing. If the FLT finds a good event, it will give a pointer (FLT-number) to this event and an FLT-accept (Fig. 9). Then the good event will be copied to the FIFO, here it is prepared for readout. The output time is digitized into an eight-bit information on the data bus for an addressed channel. The selection of a specific output channel (channel 0-7) is done by means of the channel

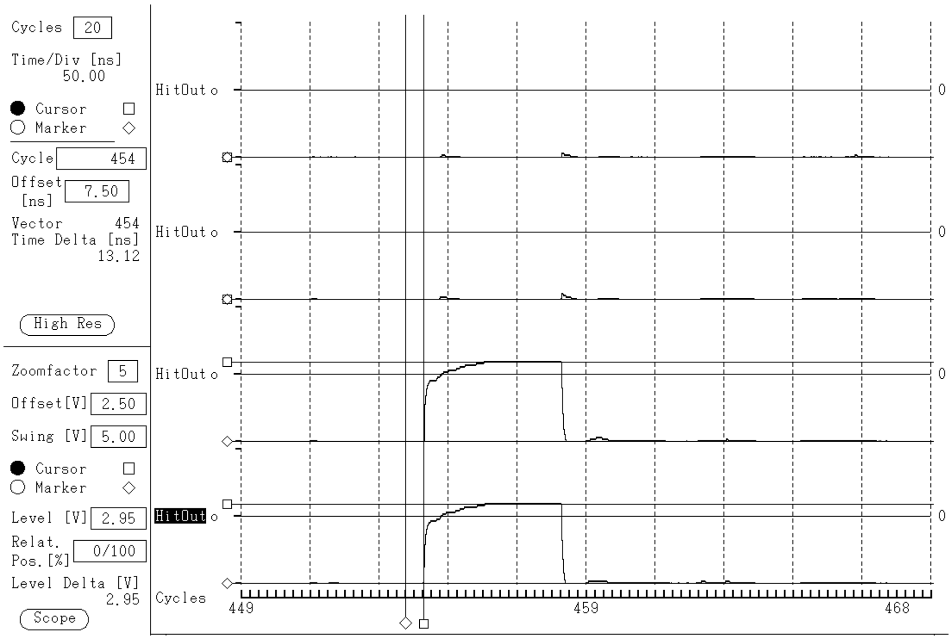

Figure 6: Here is shown the analog outputs

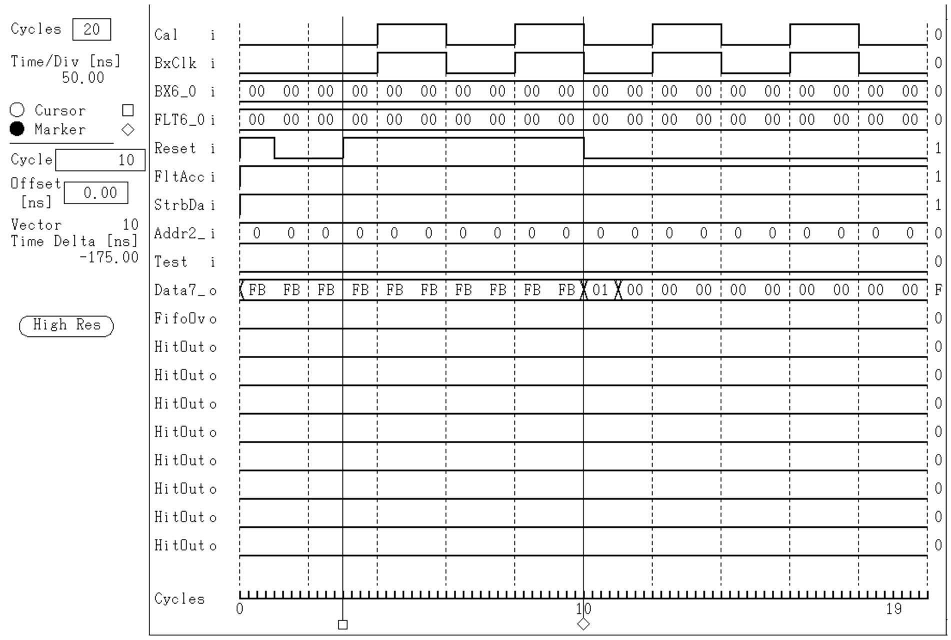

Figure 7: Presentation of the RESET signal

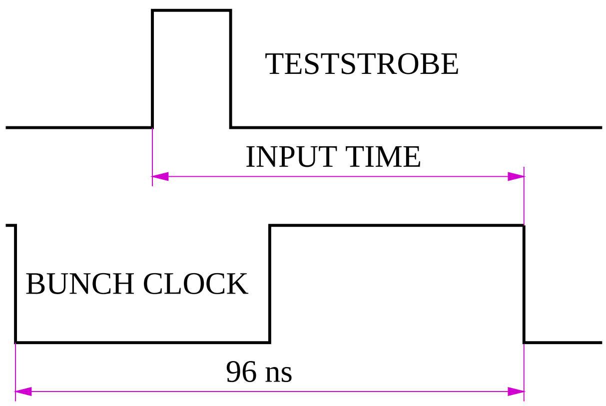

Figure 8: Presentation of the time difference

select unit (Fig. 2). A comparation of input and output time provides the result: both the times are equal inside the least-count, that means the time measurement circuit operates well. The calculation of the output time is the following:

$$t_{OUTPUT} = \frac{t_{INPUT} * 100}{256}$$

Here is t_{OUTPUT} the expected output time and t_{INPUT} the used input time.

4.3 Time measurements with GTL inputs

The GTL inputs are differential inputs for the shifted ASD8 signal (see Fig. 3). To measure with the inputs one has to:
1. enable the GTL through set PIN 46 high
2. connect the bunchclock, the calibration clock (10 MHz), FLT-Number and BX-Number
3. connect the ASD8
For the test of the differential GTL inputs the test unit was off. It generates a pulse similar to the ASD-8 output by the chip-tester. The signal is shown in figure 10. Two differential pulses (positive and negative) are needed per channel. These pulses swing around a baseline of 1,25 V with a defined height and widths (see Fig. 3). Again the input time is defined as the time difference between start and stop, with stop at the fall slope of the bunch clock. The measurements began with a swing of 160 mV and it was compared against, output with input time. Both are equal down to a pulse width of 3 ns. At less than 3 ns several channels provide false times. With a swing of 39 mV one can reach a pulse width of 8 ns. Both values are at the lower limit of the chip (that means each channel works).

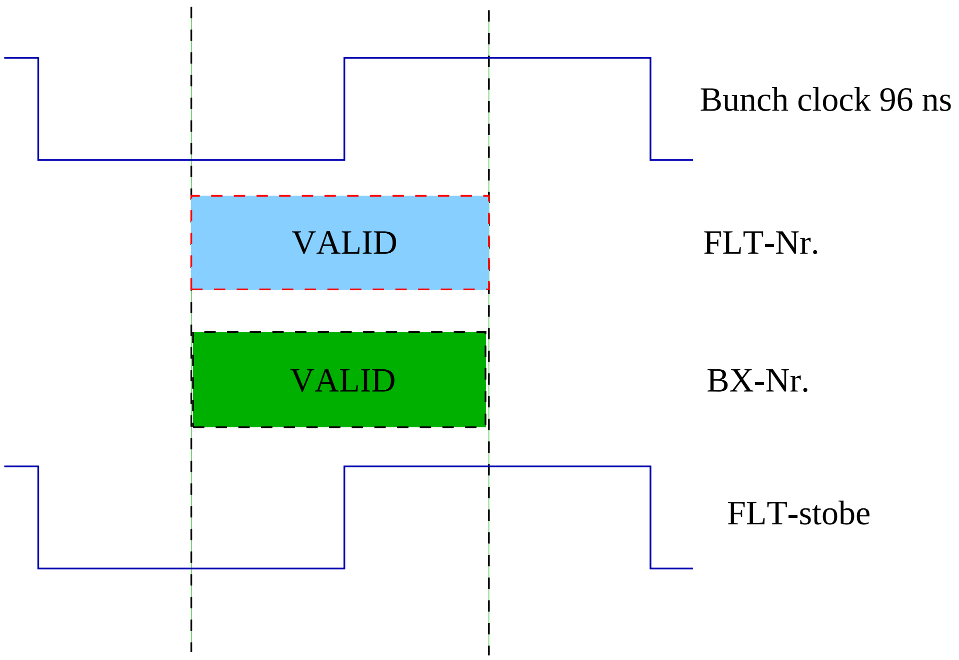

Figure 9: Timing for Buffer management

4.4 Hit registration

The TDC-Chip is also usable for hit registration, for instance to readout the muon chambers.
In that case the function bit (at PIN 24) should be HIGH. So the TDC-circuits are disabled and 64 Hit-inputs are open for measurements. The internal test-device is usable for internal hit tests too.
There is an internal buffer structure of 8 bits for storing and managing the TDC values. So 8 hit inputs are grouped together and all the buffers can be used like for the time measurements (readout see above).
In all cases the bunch clock and a BX-number must be connected. For testing the hit registration eight channels of 64 used at the same time because eight pins were available from the tester only. The three different bit pattern were necessary to check all states of all inputs (see also table 1):

11111111 for all channels
10101010 for odd channels
01010101 for even channels

The output bit pattern must equal the input bit pattern for all channels, this was

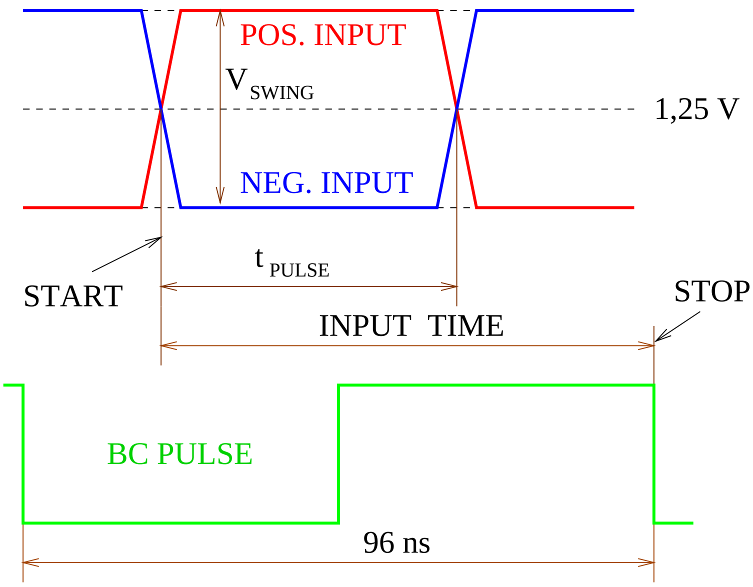

Figure 10: Scheme of the ASD8 input signal

verified in the test. The same test was made without the test unit by using the signals from the tester. In this test the minimal input pulse width was checked down to a minimum of 2 ns.

4.5 Test of pipeline

The pipeline is a data buffer, which operates in conjunction with the FLT. They work together for selecting the valid events. Therefore two different test were pattern generated for one cell (01010101 and 10101010). This test are repeated for all cell addresses (128) so the pointer management was tested by using all addresses as well as the cells themselves. By comparing the input pattern with the output pattern and it was found, that the pipeline operate without errors.

4.6 Measurement of the dead time

A important characteristic of the chip is its small dead-time. To get this we measured the whole range of the bunch clock, so we increased the input time from 0 ns to 100 ns. The result is a small dead-time at the beginning of the bunch clock of 1 ns and the end of 2 ns as shown in figure 11. This dead-time is also shown in the linearity curve in figure 12. The linearity curve presents the dependence of the output time (t_{out}) on the input time (t_{in}).

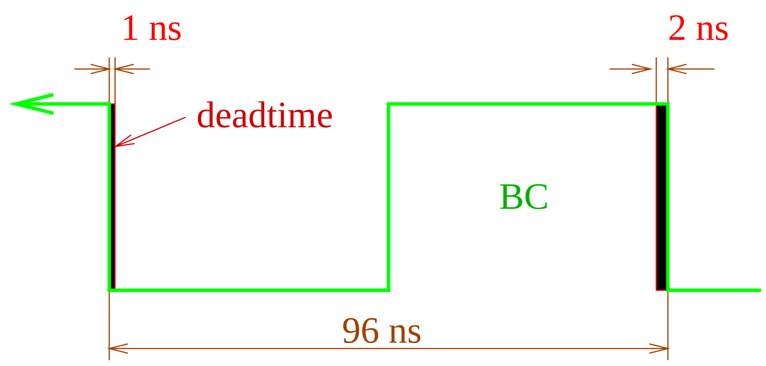

Figure 11: Dead-time of the chip

4.7 Least count measurement

In special mode one can measure directly the least count of each channel of the chip. This is necessary for controlling the time circuits.
For preparing this mode the following is done:(Fig. 13)
1. connect the BX-Clock, Calibration Clock;
2. set the test-strobe (PIN 19) HIGH;
3. put two pulses length of 20 ns on Test-input (PIN 45);
4. set the test-strobe (PIN 19) LOW;
If you set now the Hit input 0 and 1 (PIN 58/59) to high level, the output buffer will permanently give the least count of the channel. By addressing each channel you can view each circuit least count (here you don't need any read-strobe [read above]).
The raw least count you have now contains the first 8 of 10 Bits of the offset free eichwert. The lower 2 bits have no significance, so they were shifted left by multiplying by four. This gives you the value of quantization steps for a period of 100 ns. If you divide 100 by the number of steps you get the intern least-count. For optimization of the differential nonlinearity two quantization steps were grouped together. The result is the real least-count.

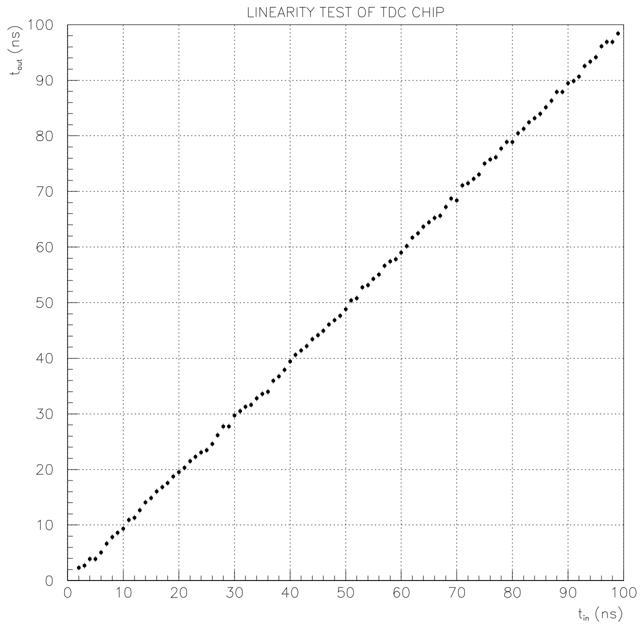

Figure 12: Result of the linearity test

Example for calculating the real least-count in [ns] from raw least-count:

$$\text{read least count} \qquad (0x75 \text{ hex}) = 115$$
$$115 * 4 = 460 \qquad (\text{shift left to get a 10 bit value from 8 bit})$$
$$\text{this is the number of quantization steps for 100 ns}$$
$$\frac{100}{460} = 0.2174 \qquad \text{internal least count}$$
$$\rightsquigarrow 0.2174 \cdot 2 = .4348 \qquad \text{REAL LEAST COUNT}$$

The least count of the chip is per description 0.5 ns. The time measurement is realized by 8 bits, one has 256 time channels and this is related to 128 ns. But in the experiment there will be a maximal drift time of $\tau_{Drift}^{max} =\simeq 70$ ns. So the 8 bit are sufficient for the time measurement. At room-temperature a least-count of 0.45 ns was obtained. The dependence of the least-count on the temperature was also found. The theoretical factor of these dependence is ≈ 0.3 % per degree. In table 4 are some measured values

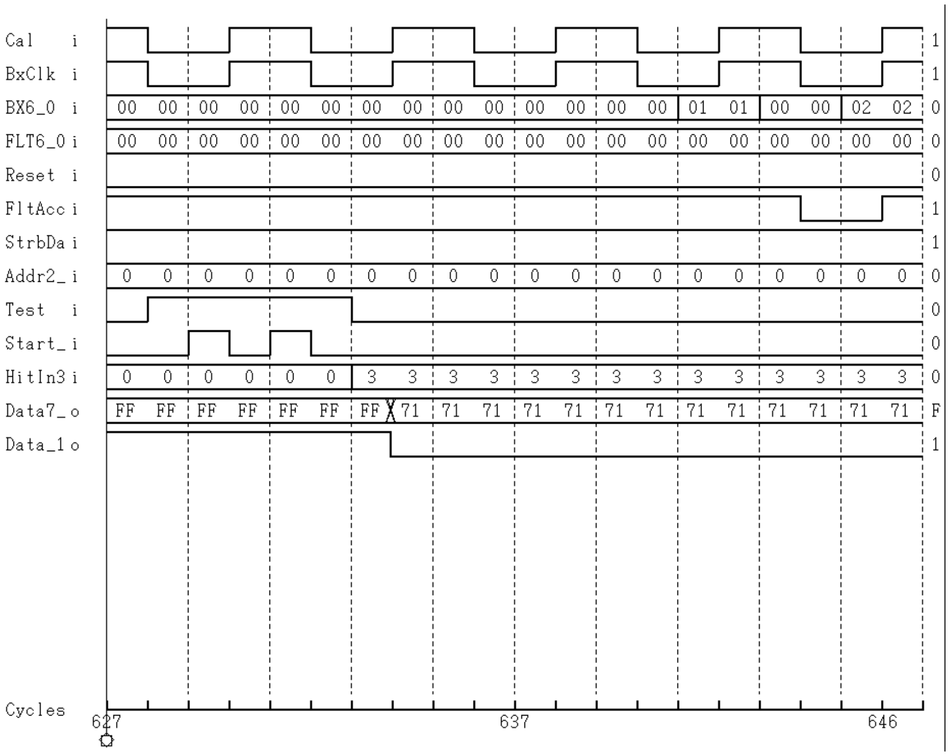

Figure 13: Get the chip into the special mode

25 °C	0,451 ns
0 °C	0,416 ns
-10 °C	0,4032 ns

Table 4: Least-count dependence of the temperature

of the temperature dependence. In addition the least-count dependence on the power voltage, so we need a stabilized power supply. The dependence on the temperature corrects the chip itself (see 2.2.4).