Priority	Task	Short	availlable [manmonth] Phys	availlable [manmonth] Techn	required [manmonth] Phys	required [manmonth] Techn	Start	Status Updated	Done [%]	Resources	Estimated duration [days]	Done at	Who	Stone
	Total		**97.9**	**10**	**30**	**13**	**1/6/00**					**14/3/02**		
		Online:	10.15	0	11	6	**1/12/00**					**14/3/02**		
1	Integrate High–Pt (LUTs, Setup, Simulation, Tests)	High–Pt			6						186			
4	Client Library upgrade	FLTDesk	0.1				**1/1/01**			0.1	31	**31/1/01**	AM	
4	slow control of temperatures	temperature SC	1				**1/3/01**			0.3	102	**10/6/01**	AM	
4	upgrade of TxU board control programs	board software	0.6				**1/12/00**			0.3	61	**31/1/01**	AM	
3	integrated setup database	setup DB			1						31			
4	improve reliability and speed of RPF	RPF upgrade	0.2				**1/12/00**			0.1	61	**31/1/01**	AM	
3	system monitoring	monitoring	3				**1/3/01**			0.8	114	**23/6/01**	IR	
4	network wide re–processing of events	network vector test	1				**1/2/01**			0.4	76	**18/4/01**	AM+IR	18/4/01
3	upgrade of formatter	formatter	0.25				**1/1/01**			0.25	31	**31/1/01**	DR	
4	Board tests	board tests	1		3		**1/2/01**			0.3	407	**14/3/02**	AM+??	
3	Interface to Pretriggers and debug connections	Pretrigger IF			3					0.1	915			
4	event by Event Comaprison of detector and trigger link data	Event By Event			2		**10/1/01**			2	31	**9/2/01**	XW,BS,DR	
5	Upgrade message repeaters/message boards/multiplexers	repeaters	3		1	3	**1/2/01**			3	71	**13/4/01**	Ma+DESY technicians	
	Upgrade of Message Board Library for new features	Message Library			0.5						15			
3	Debugging of PECL Splitter	PECL splitter			0.5						15			
4	Upgrade TFUs opto receivers	TFU receiiver upgrade				3	**1/3/01**			2	46	**15/4/01**	Ma Hiwis	
		Tooling:	9	0	3	0	**15/10/00**					**8/4/01**		
3	Interface DB to hera–b standard (allow for versioning and access by any user).	Data Base IF	1		3						122		IN	
5	Improve simulation (link masking, mapping defects, hot/dead channel lists, latency and message overflow conditions, run based DB setup).	Simulation update	4				**15/10/00**	5/12/00	75	1.3	75	**28/12/00**	IR, DR	
4	Impelement simulation into ARTE and release to general hera–b user	ARTE Integration	4				**15/10/00**	5/12/00	50	0.5	175	**8/4/01**	MN, HF	

		Analysis:	32	0	0	0	**1/6/00**					**16/7/01**		
4	Understand “minor” HW issues (tranparent mode screw up, TDU bit errors)	HW issues	2				**16/3/01**			0.5	122	**16/7/01**	IR	
5	Understand EPre efficiency and do realistic Simulation.	EPRE efficiency	4				**1/6/00**			0.5	244	**31/1/01**	JF	
5	Understand online/simulation deviation (data link problems, correlation with real tracks, message overflow problems).	Online/Simu Comparison	5				**1/10/00**				153	**2/3/01**	BS	
5	Estimate e efficiency based on reference tracks.	E reference track	2				**1/9/00**			0.5	122	**1/1/01**	MB	
5	Estimate mu efficiency based on reference tracks.	Mu ref. Track	2				**1/9/00**			0.5	122	**1/1/01**	AS	
4	Estimate single track efficiency from J/Psis using single lepton triggered events.	Mu track eff from J/Psi	3				**28/12/00**	1/1/01	20	1	78	**16/3/01**	TN, IR	**16/3/01**
4	Understand pair trigger efficiency for J/Psis.	understand pair trigger	2				**10/1/01**			0.33	185	**13/7/01**	DR	**13/7/01**
4	study muon latency in Simulation, influence of link masking, study pileup	muon latency study	1					7/12/00	30	1	21			
5	Understand MU1 inefficiency (run simulation on hard selected SLT J/Psis and find reasons for not found SLT tracks).	MU1 inefficiency	4				**1/10/00**	14/12/00	40	0.9	157	**6/3/01**	HF	**6/3/01**
4	try to remove MU4 to reduce latency	MU4 removal	2				**6/3/01**			1	61	**6/5/01**	HF	
4	minimize RoIs to minimize clones and optimize latency	RoI Optimization	1							1	31			
5	Understand alignment effects, evtl. upgrade LUTs to include realistic geometry.	realistic Geo LUTs	3							1	92			
2	Understand reasons for too small Mass/P from TPU: check Py binning!	TPU reco.	1				**31/1/01**			0.2	153	**2/7/01**	JF	
		Algorithm Upgrades:	0	0	13	0	**2/7/01**					**2/12/01**		
3	Mapping of Inner Tracker	ITR Mapping			1						31			
2	Mapping of Pixel	Pixel Mapping			1						31			
3	Update Mapping of OTR	OTR Mappiung Update			2						61			
3	Upgrade TFUs for missing hits (incl. simulation)	TFU hit ommiting			2						61		Ma+??	
1	Upgrade TPUs double track rejection (incl. simulation)	TPU double track			1		**2/7/01**			0.2	153	**2/12/01**	Ma+JF	
3	Upgrade TFU algorithm for ITR	ITR Algorithm			2						61			
2	Upgrade TFU algorithm for pixels	Pixel Algorithm			2						61			
3	ITR Tracking comissioning with 2001/2002 data	ITR Tracking comissioning			1						31			
2	Pixel Tracking comissioning with 2001/2002 data	Pixel Tracking comissioning			1						31			

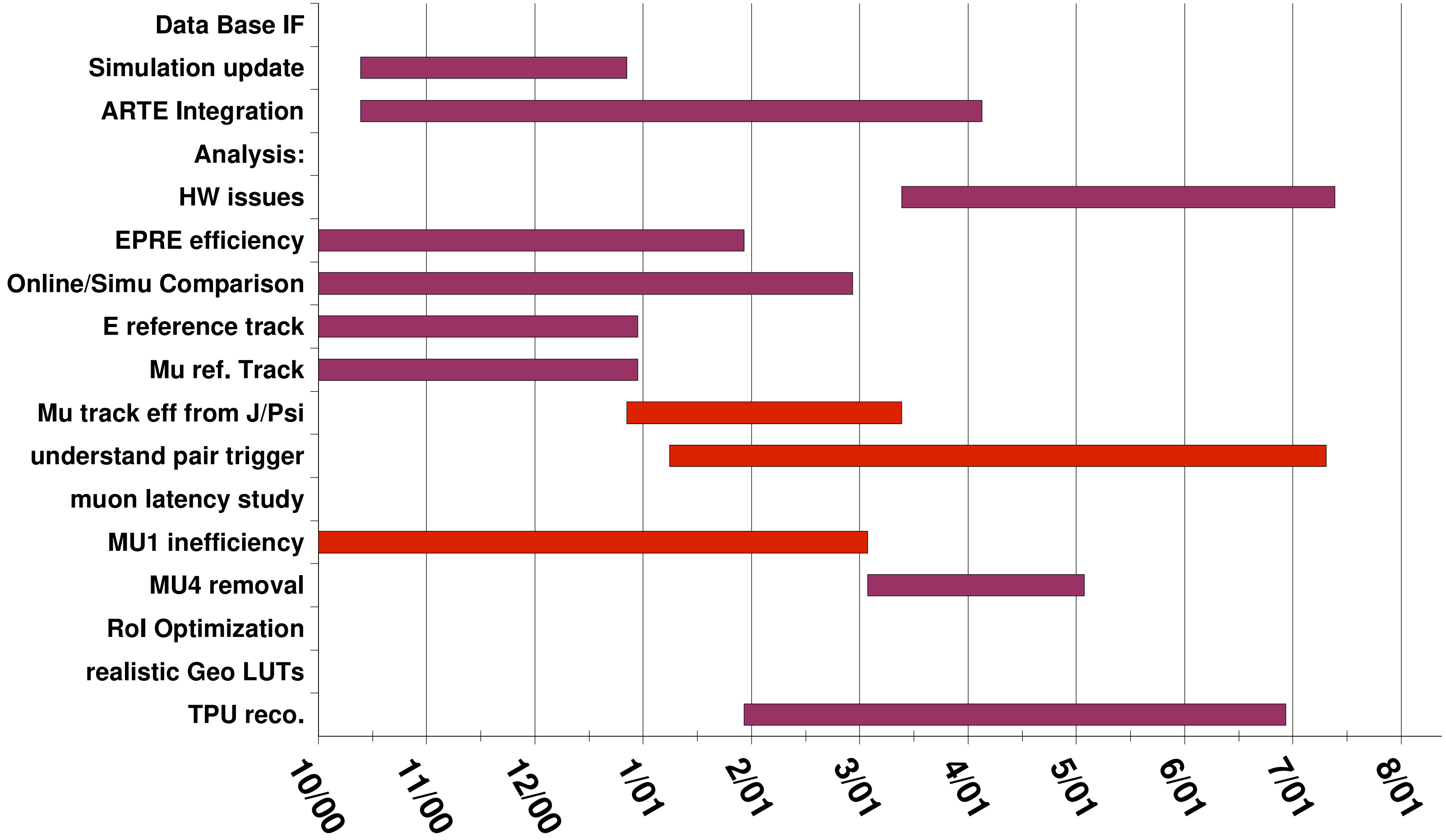
		Link Boards:	11	4	0	7	**1/9/00**					**31/8/01**	Ma Hiwis	
5	Implementation of remote adjustment of offset and bias currents for optical transmitters, including VME interface for I2C bus; production of piggy bag PCB and modificatioj of transmitter	remote offsets	2	2		3	**1/9/00**			1	214	**2/4/01**	Uni−HH, Mannheim	
5	Improve test procedure during installation (ensure low bit error of transmission line)	test procedure	1				**1/1/01**			1	31	**31/1/01**	Xiaowei+Bernhard	
3	Implement a register on the PLDs which is accessible via FCS strobes to mask dead channels	EPLD channel masks	1				**1/2/01**			1	31	**3/3/01**	Xiaowei+Bernhard	
4	Re−Installation and cabling of LinkBoards	re−cabling		1			**1/5/01**				31	**31/5/01**		**31/5/01**
4	Improve cabling of LinkBoards (extention PCB for LinkBoard for easier access to connectors)	better cabling	1			2	**1/1/01**			0.75	122	**3/5/01**	Wurth, MSC	
4	Improve cooling of AutoBahn chips on LinkBoard	Link Board cooling	1	1		2	**1/1/01**			0.8	153	**2/6/01**	Ekkehard+Kai	
5	Checking of cabling after installation	check cabling	4				**1/5/01**			1	122	**31/8/01**	Xiaowei	**31/8/01**
3	Commissioning of Pixel Mapping Boards	Pixel Mapping Board	1								31		Bernhard+Xiaowei	
		e Pretrigger:	7	6	1	0	**1/7/00**					**7/31/01**		
	Decrease bit error rate (Install ECAL Readout in Mai)	Bit errors	1	2			**1/7/01**			3	31	**31/7/01**		**31/7/01**
	Bremsstrahlungs recovery system upgrade	Brem Upgrade		1			**1/1/01**			1	31	**31/1/01**		
	Develop Bremsstrahlungs test procedure	Brem Test Development	1				**31/1/01**				31	**3/3/01**		
	Test Bremstrahlungsrecovery	Brem Test		3			**3/3/01**				92	**2/6/01**		
	Pretrigger rate monitor	HW Rate Monitor	1				**1/3/01**			0.3	102	**10/6/01**		
	EPRE Simulation Match	Simulation match	4				**1/7/00**	1/12/00	100	1	153	**1/12/00**		
	Understand Pretrigger Rate and Efficiency in 2000: J/Psi disapearing??	Understand run 2000			1						31			
	Lab test and comission Ecal Inhibt Card and deliver to DESY	EEI lab test		3			**1/12/00**				92	**2/3/01**		**2/3/01**
	Comissioning of Ecal Inhibt Card at DESY	EEI comissioning			2						61			
		m Pretrigger:	52.5	0	4	0	**1/11/00**					**6/2/01**		
5	Improve mechanical fixations of POLs to PLBs	POL Mechanics		1				13/12/00	90		3			
5	Repair PLBs	PLB Repair		1				13/12/00	00		31			
5	Repair PCUs	PCU Repair		1				13/12/00	80		6			
5	PMB debugging	PMB debugging	1	1				13/12/00	25		46			
4	Improve optical link reliability by installation of remote adjustment of offset and bias currents for optical transmitters	remote POL	2	6				13/12/00	00		244			
3	Improve monitoring software	Monitoriung Software	6					13/12/00	10		165			
2	Produce additional spare modules	Spare produciton	1	4				13/12/00	00		153			
	Repair and Test of all Systems in Dortmund	Repair and Lab−Test	10	14			**1/9/00**			3.05	240	**29/4/01**		
5	Reinstall full System at DESY	Reinstallation	2				**1/5/01**			4	15	**16/5/01**		**16/5/01**
5	Re−commissioning	Recomisisoning	2				**16/5/01**			2	31	**15/6/01**		**15/6/01**

	SLT:	28.75	0	2	0	**1/11/00**					**6/2/01**	
5	ITR−integration	ITR−integration	2			**7/11/00**	7/12/00	50	1	61	**7/1/01**	PK,TN
5	ITR−RoI sparsification	ITR−RoI sparsification		2					1	62		
5	CnA: introduce ITR l2maps	ITR−maps via CnA	0.5			**7/11/00**	7/12/00	100	0.25	30	**7/12/00**	PK
5	L2−Magnet: RoI handling	L2−Magnet	4			**1/11/00**	1/12/00	20	0.66	180	**30/4/01**	RM
5	Refit: introduce OTR calibration via CnA and add drift time	Refit drift time	1			**1/1/01**			0.5	62	**4/3/01**	PK
3	L2Sili: multiple scattering treatment and timing optimization	L2Sili upgrade	5			**15/1/01**			1.2	129	**24/5/01**	BP,RM
3	L2Vertex: finalize output	L2Vertex finalization	0.25			**14/5/01**			1	8	**21/5/01**	BP
4	SLT: algorithm timing optimization	SLT algo timing	2			**1/4/01**			1	62	**2/6/01**	TN
3	MAP/PAM: optimization	MAP/PAM	2			**15/2/01**			0.75	83	**8/5/01**	LS
3	FLT−SLT interface: finalize and test	FLT−SLT interface	0.5			**7/1/01**			0.25	62	**10/3/01**	TN
3	Trigger type handling: implement as CnA client, formatter	Trigger Type handling	1			**1/11/00**	1/12/00	100	1	30	**1/12/00**	TN
4	SLT−2000 Analysis: efficiency, reduction, timing	SLT−2000 Analysis	4			**1/11/00**	1/12/00	25	1	123	**4/3/01**	All
3	SLT−Arte support: maintain and develop sltinfo + tools	SLT−ARTE support	1.5			**1/11/00**	1/12/00	75	0.1	146	**27/3/01**	BP
4	MC−DAQif: switch to OTRi, include ITR, maintenance	MC−Daqif	2.5			**1/11/00**	15/12/00	75	0.75	70	**9/1/01**	LS
4	MC−DSLT production.	MC−DSLT production	1.75			**8/11/00**	1/12/00	25	0.25	186	**12/5/01**	LS
2	SLT code management	SLT code management	0.75			**1/11/00**	1/12/00	30	0.1	193	**12/5/01**	BP

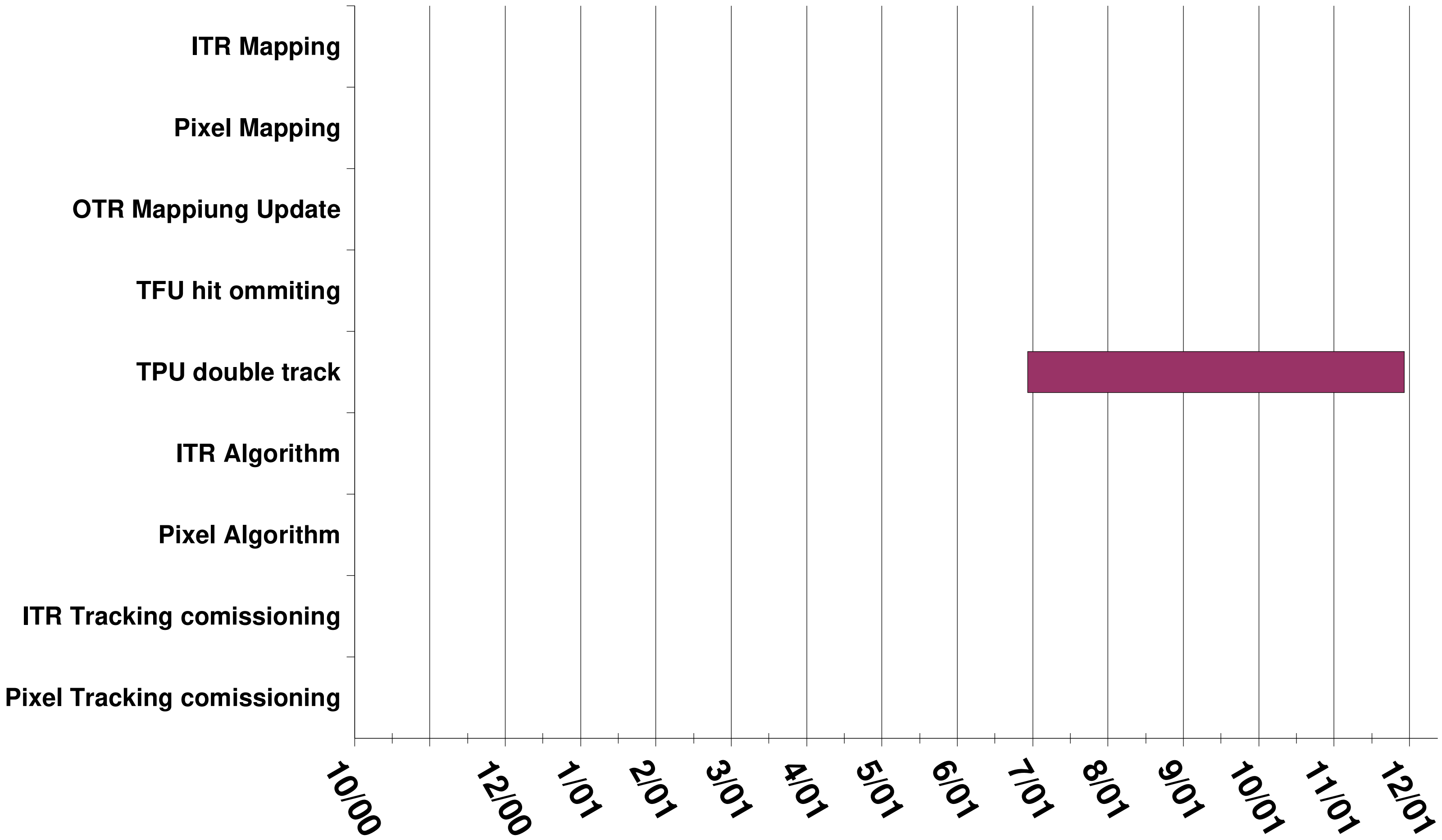
FLT Online


High–Pt
FLTDesk
temperature SC
board software
setup DB
RPF upgrade
monitoring
network vector test
formatter
board tests
Pretrigger IF
Event By Event
repeaters
Message Library
PECL splitter
TFU receiiver upgrade
10/00
12/00
2/01
3/01
4/01
5/01
6/01
7/01
8/01
9/01
11/01
1/02
2/02
3/02

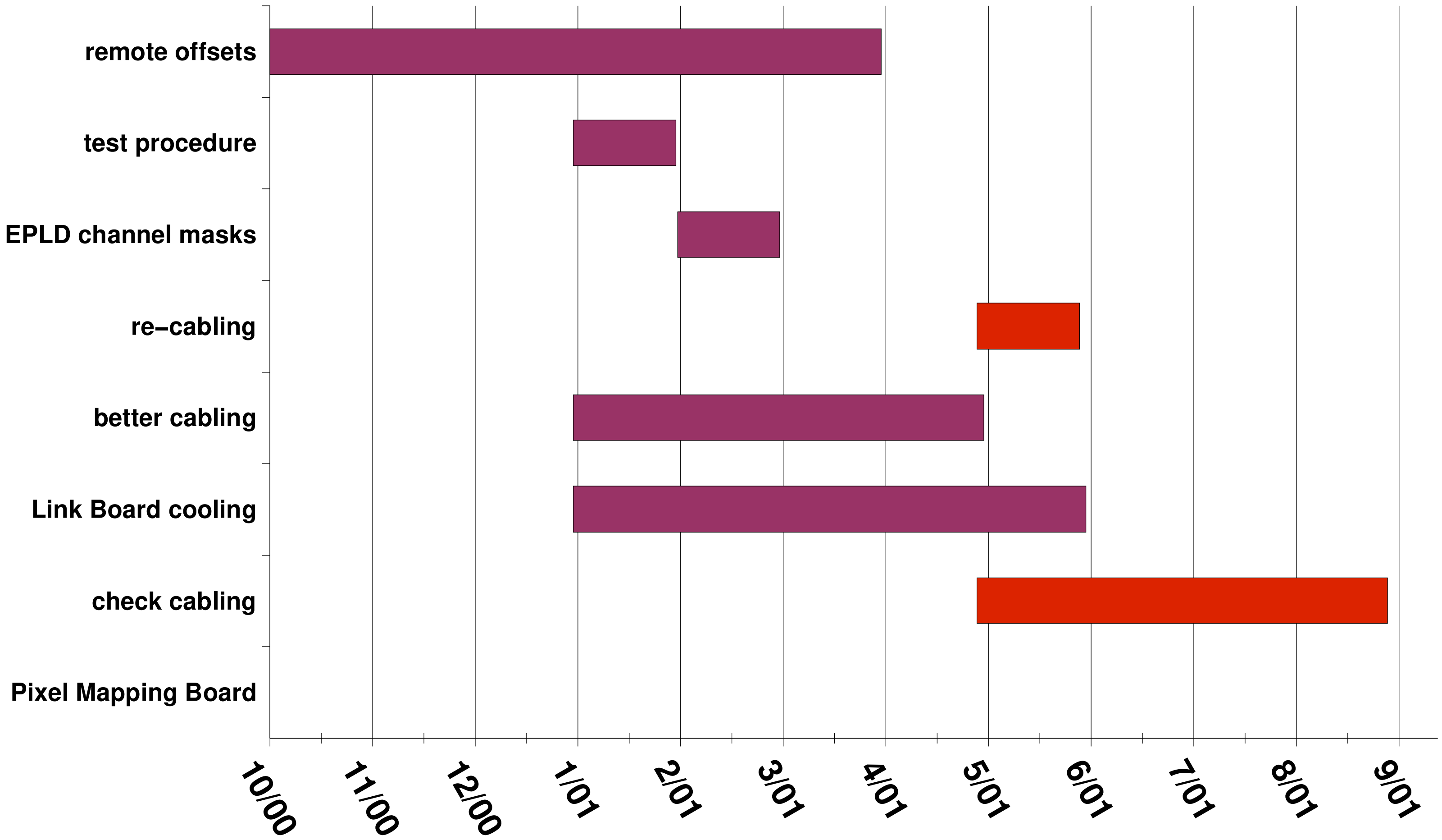
FLT Tooling and Analysis



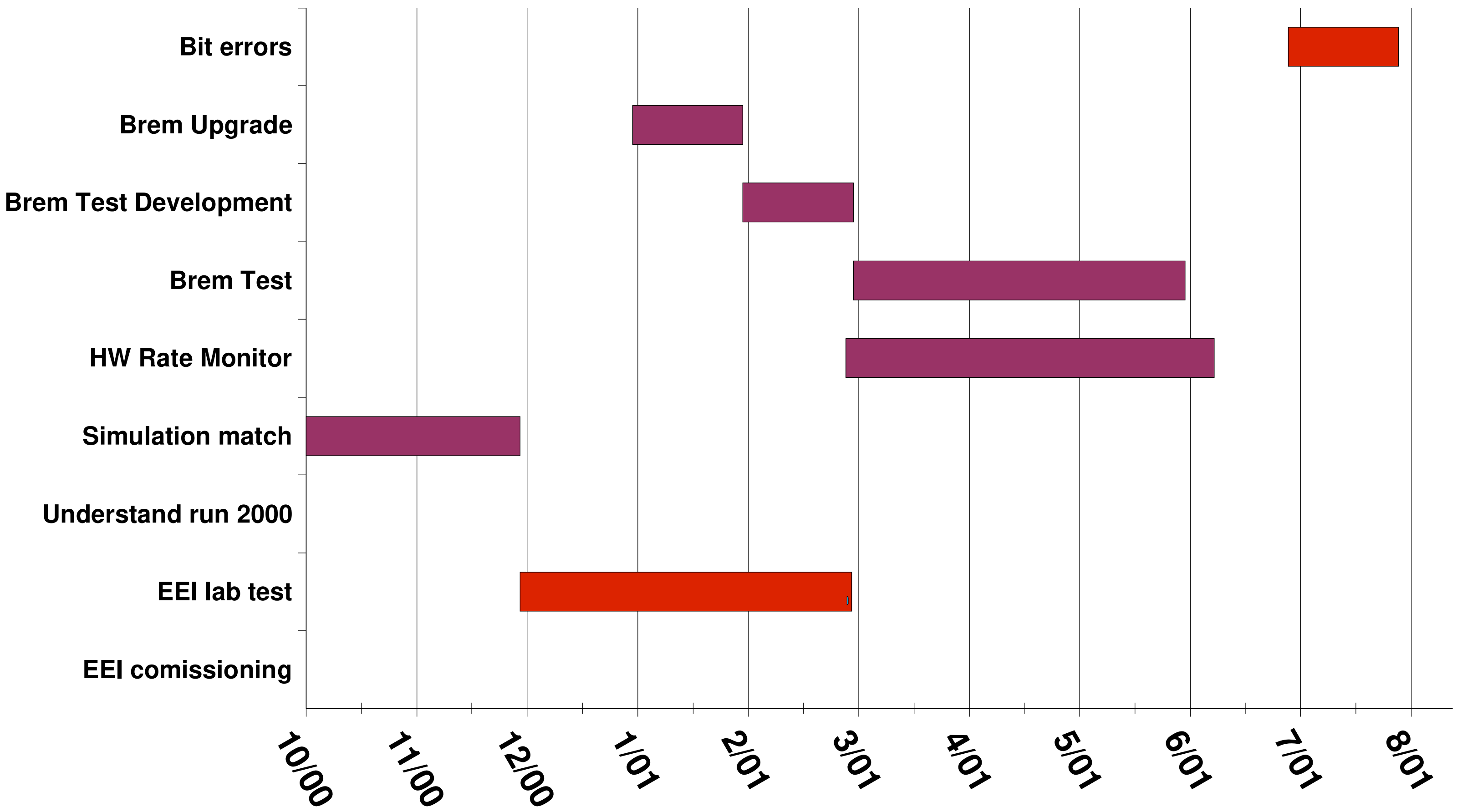
Algorithm updates



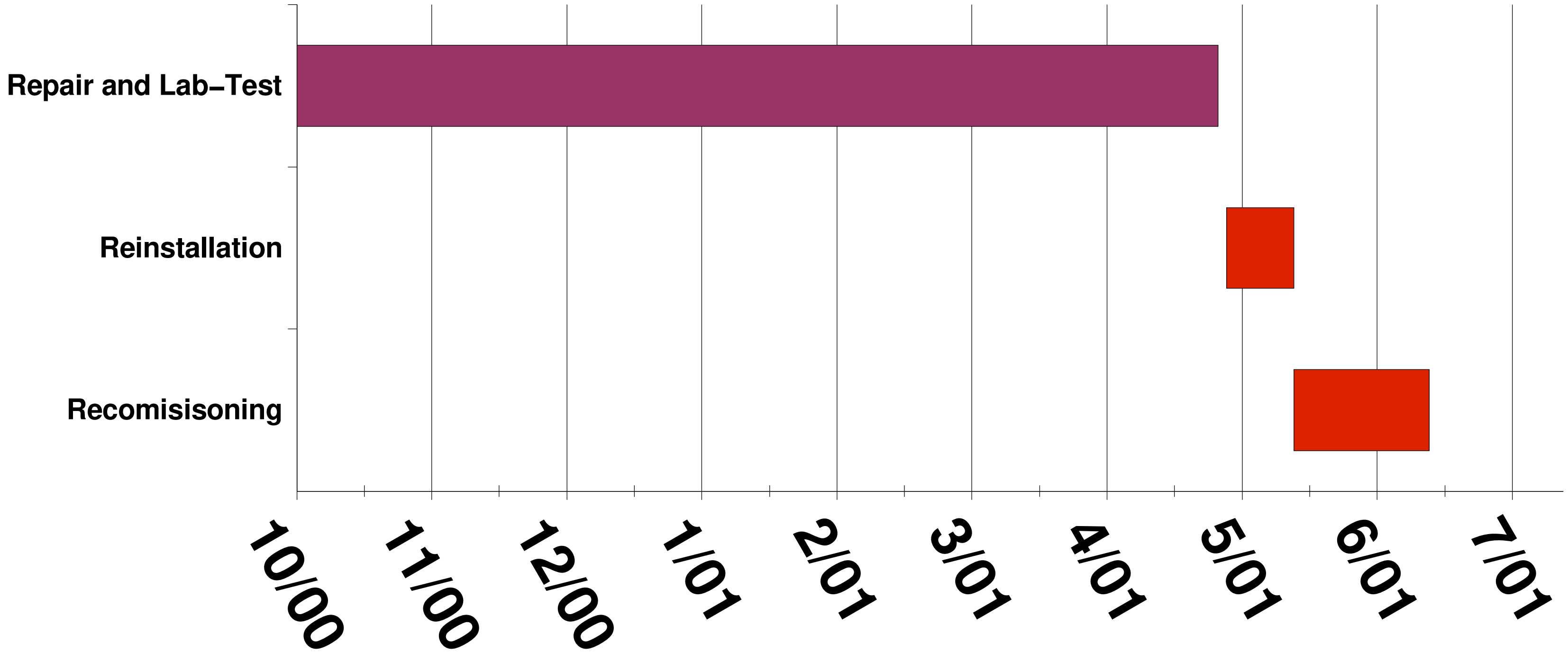
Link Boards

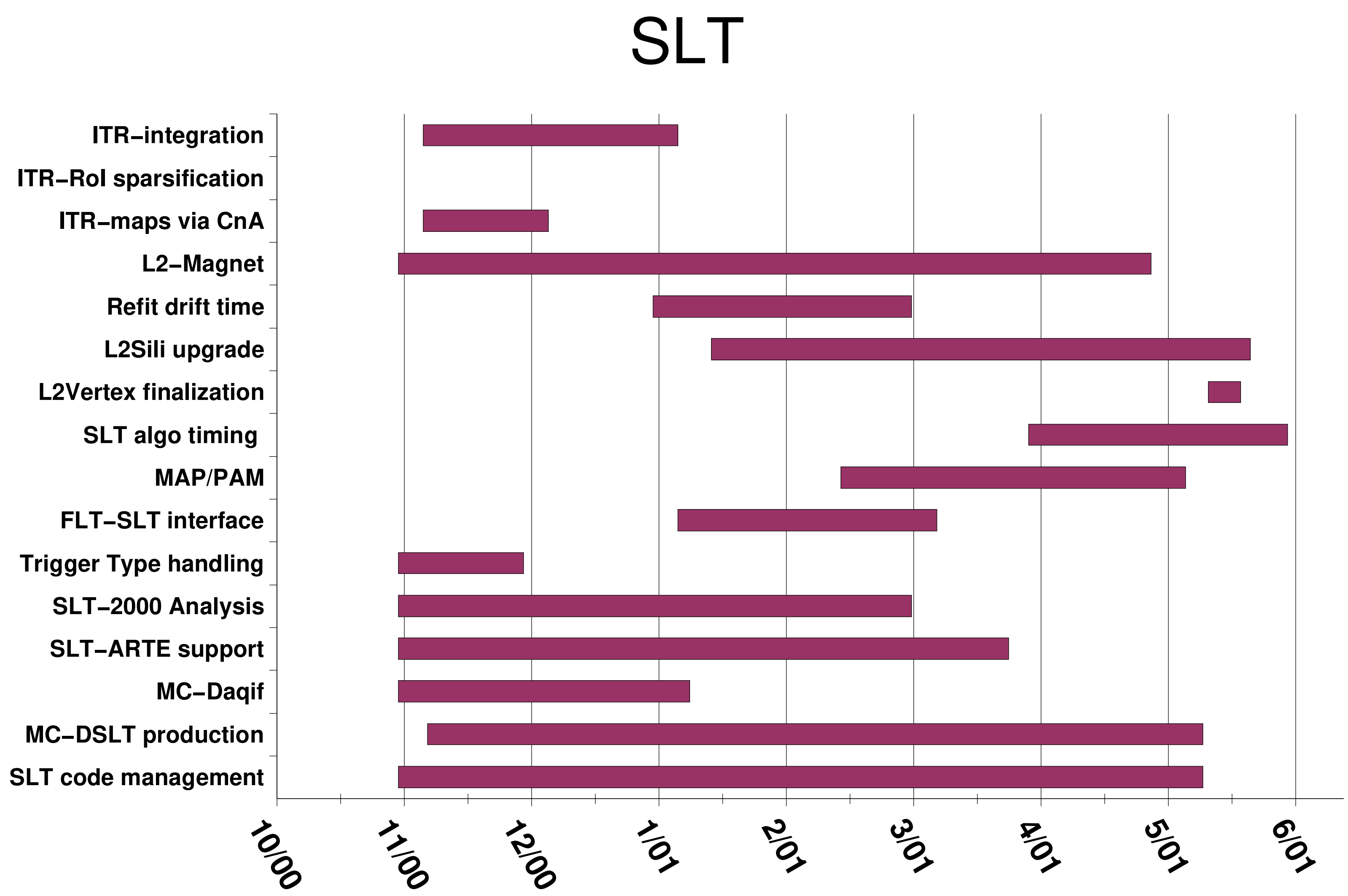

remote offsets
test procedure
EPLD channel masks
re−cabling
better cabling
Link Board cooling
check cabling
Pixel Mapping Board
10/00
11/00
12/00
1/01
2/01
3/01
4/01
5/01
6/01
7/01
8/01
9/01

E Pretrigger

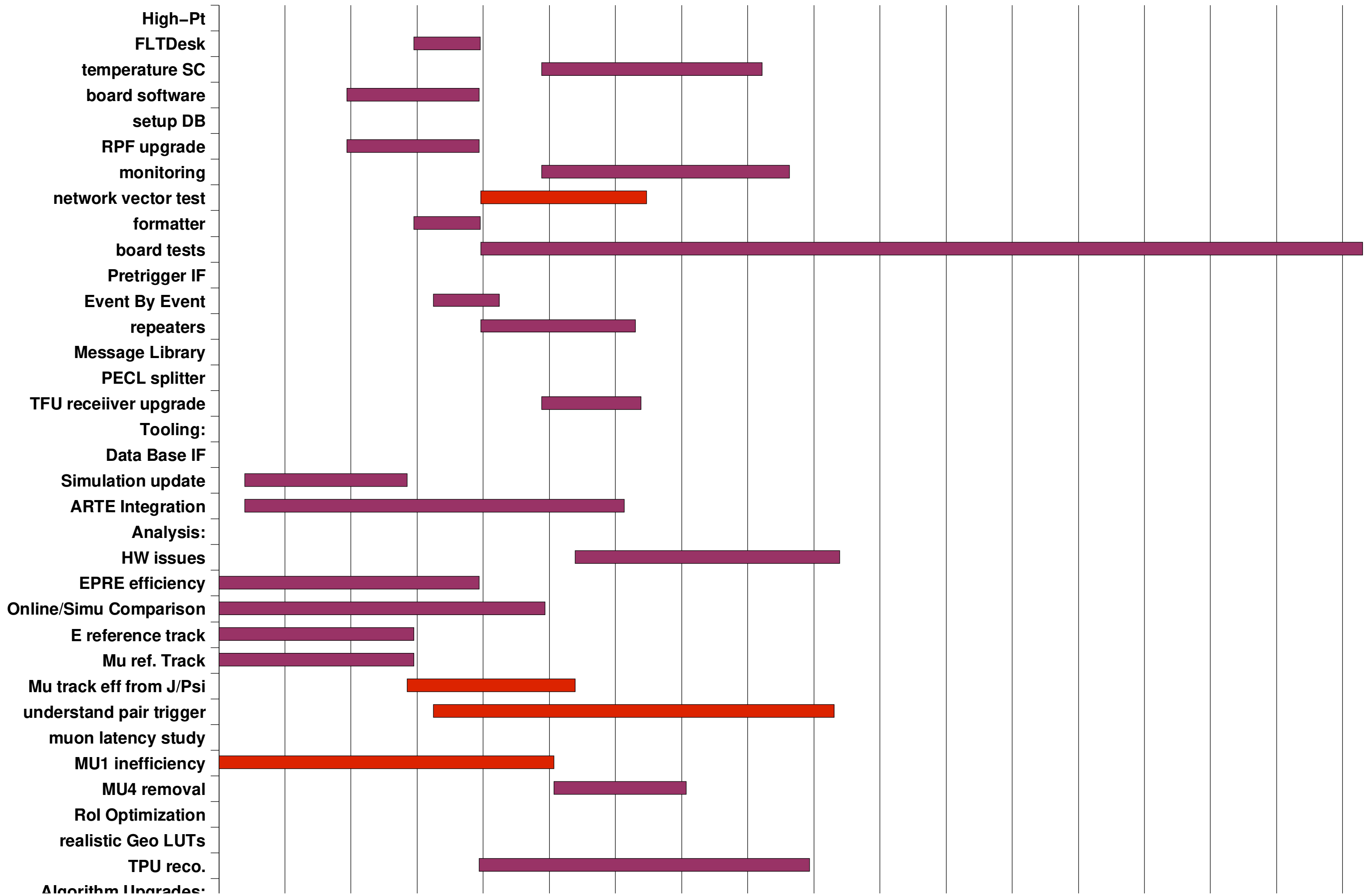


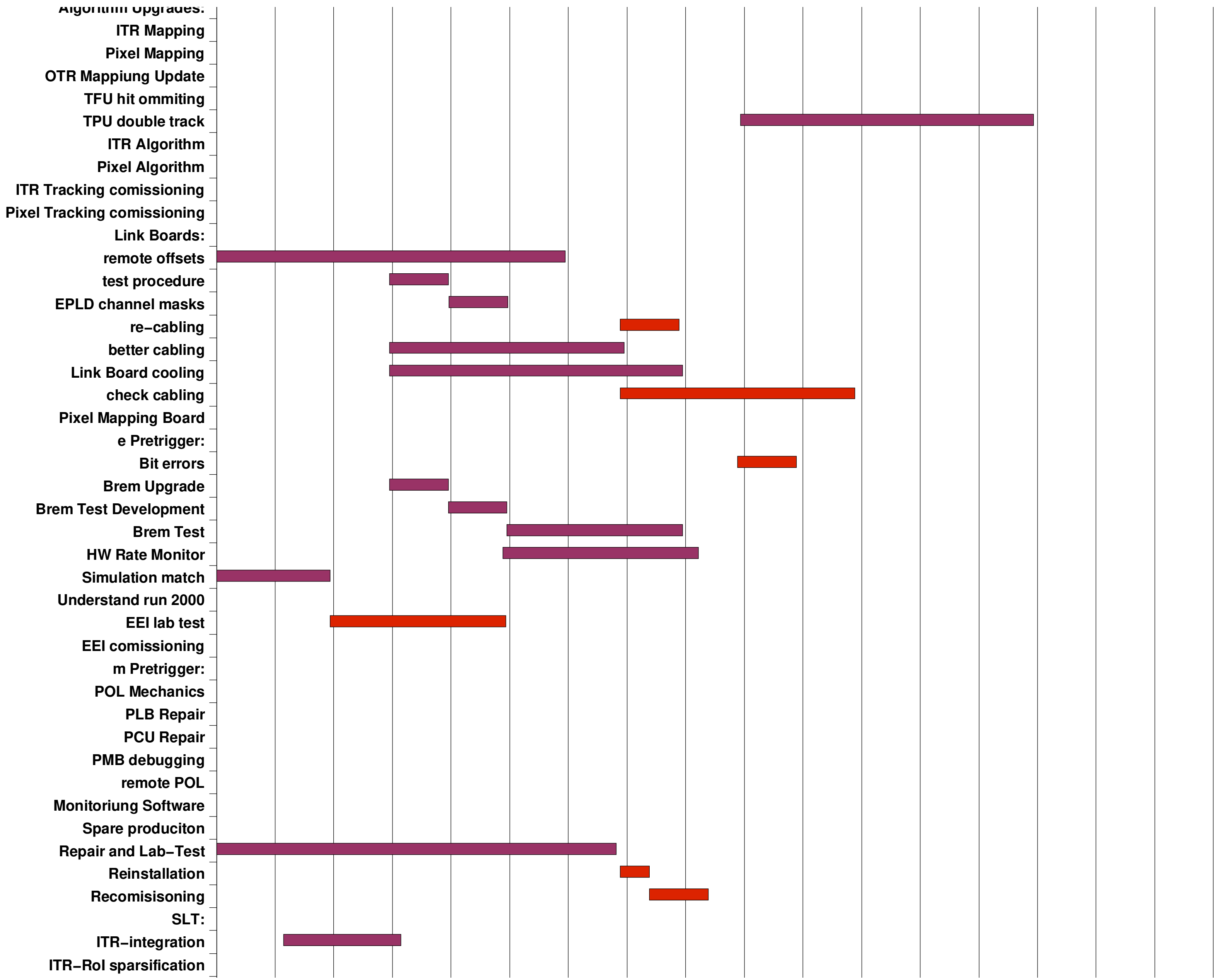
muon Pretrigger

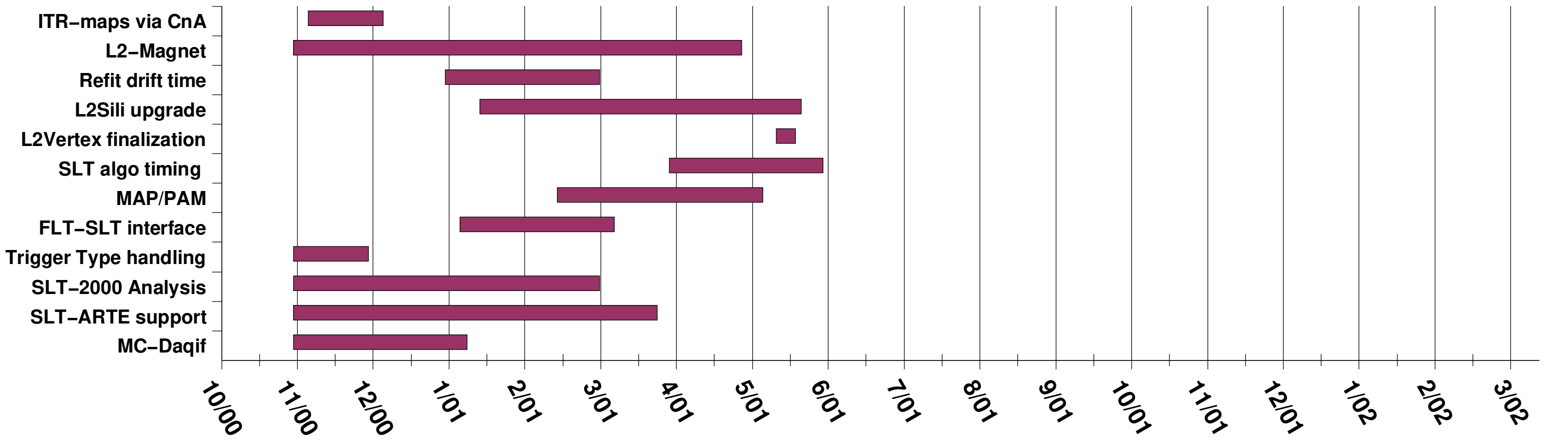



SLT
ITR–integration
ITR–RoI sparsification
ITR–maps via CnA
L2–Magnet
Refit drift time
L2Sili upgrade
L2Vertex finalization
SLT algo timing
MAP/PAM
FLT–SLT interface
Trigger Type handling
SLT–2000 Analysis
SLT–ARTE support
MC–Daqif
MC–DSLT production
SLT code management
10/00
11/00
12/00
1/01
2/01
3/01
4/01
5/01
6/01

All Trigger Tasks




Algorithm Upgrades:
ITR Mapping
Pixel Mapping
OTR Mappiung Update
TFU hit ommiting
TPU double track
ITR Algorithm
Pixel Algorithm
ITR Tracking comissioning
Pixel Tracking comissioning
Link Boards:
remote offsets
test procedure
EPLD channel masks
re–cabling
better cabling
Link Board cooling
check cabling
Pixel Mapping Board
e Pretrigger:
Bit errors
Brem Upgrade
Brem Test Development
Brem Test
HW Rate Monitor
Simulation match
Understand run 2000
EEI lab test
EEI comissioning
m Pretrigger:
POL Mechanics
PLB Repair
PCU Repair
PMB debugging
remote POL
Monitoriung Software
Spare produciton
Repair and Lab–Test
Reinstallation
Recomisisoning
SLT:
ITR–integration
ITR–RoI sparsification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10/00
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