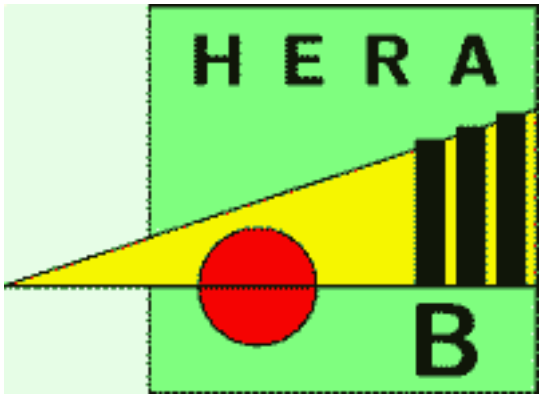



FLT

# Hardware FLTSIM Run '98

**12 - June - 1998**

**Ekkehard K E Gerndt, DESY**

# FLT network overview I

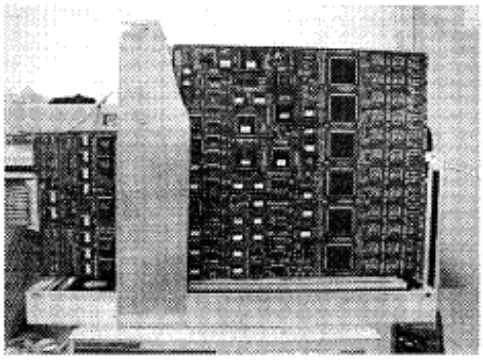
| TFU test series | 2 | 8 | |
|---|---|---|---|
| layout | ✔ | ✔ | |
| PCBs | ✔ | ✔ | |
| WIMs | ✔ | ✔ | ← ∀ TFUs !! |
| Autobahns | ✔ | ✔ | ← comment |
| other ICs | ✔ | ordered | |
| optical links | ✔ | open | |
| assembly | 1.5 | | |
| FLTSIM test | ✔ | | |

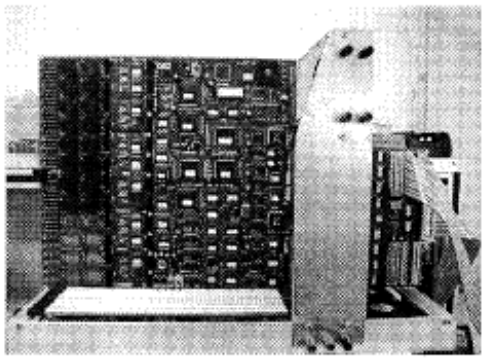
➜ first TFU @ DESY 1 Aug. '98
➜ remaining 8 TFUs 1 Oct. … Nov. '98

| TPU | 2 |
|---|---|
| layout | ✔ |
| PCBs | ✔ |
| ICs | ✔ |
| assembly | ✔ |
| FLTSIM test | |

➜ one TPU @ DESY 24 June '98

# Track Finding Unit





Timing problems of version 1 fixed in version 2.
Different pinout of WIM ASIC fixed in version 2.

1st prototyp assembled and tested.
2nd prototyp will be assembled in Mannheim.
Small series (TFU#3 to #10):
- IC's are ordered.
- Mounting will be done by indutrie.
- Production will start soon.

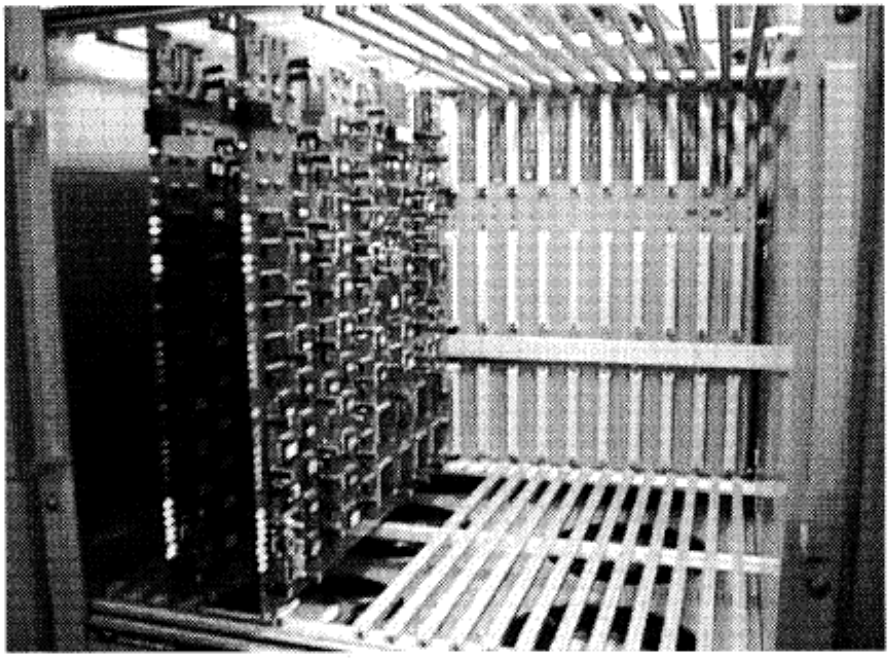
Crosscheck with FLTSIM done.

## Message Board:

Redesign ready for 10-series.
- Better timing of the 100 MHz clock and control signals.
- All PLDs in circuit programmable.

Joachim Gläß, Informatik V, Univ. Mannheim, email: glaess@ti.uni-mannheim.de

# Track Parameter Unit



2 boards assembled and tested

to do:
crosscheck with FLTSIM

Joachim Gläß, Informatik V, Univ. Mannheim, email: glaess@ti.uni-mannheim.de

# FLT network overview II

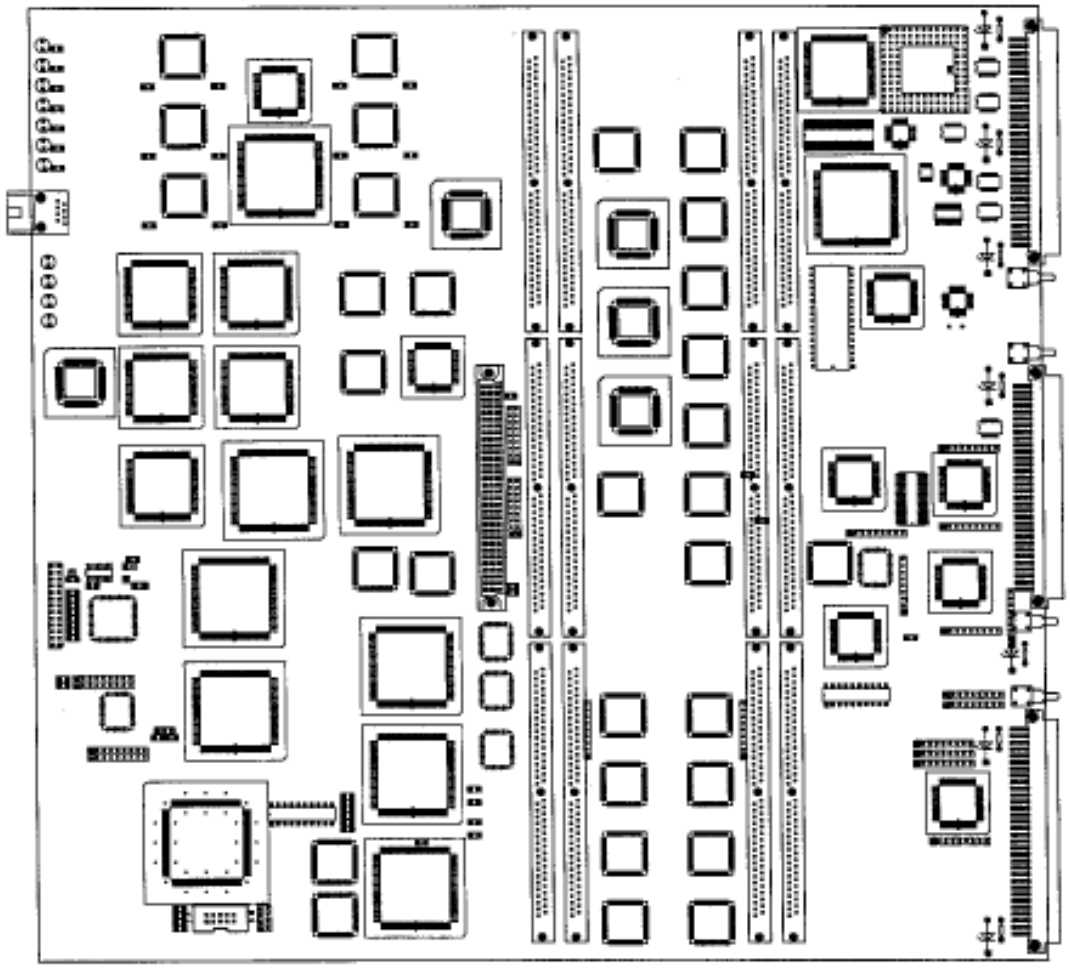
| Test Board | 2 |
|---|---|
| layout | ✔ |
| PCBs | ✔ |
| ICs | ✔ |
| assembly | ✔ |

➜ refurbished Test Board back 15 July '98

| TDU prototype | 1 |
|---|---|
| LUT subcard layout | ✔ |
| layout | SHARC link & CPU ctrl missing |
| PCB | |
| ICs | some |
| assembly | |
| FLTSIM test | |

➜ TDU with reduced capability @ 7 Oct. '98

# Trigger Decision Unit



LUT subcard connectors

PCB layout in work

**LUT subcard layout finished**

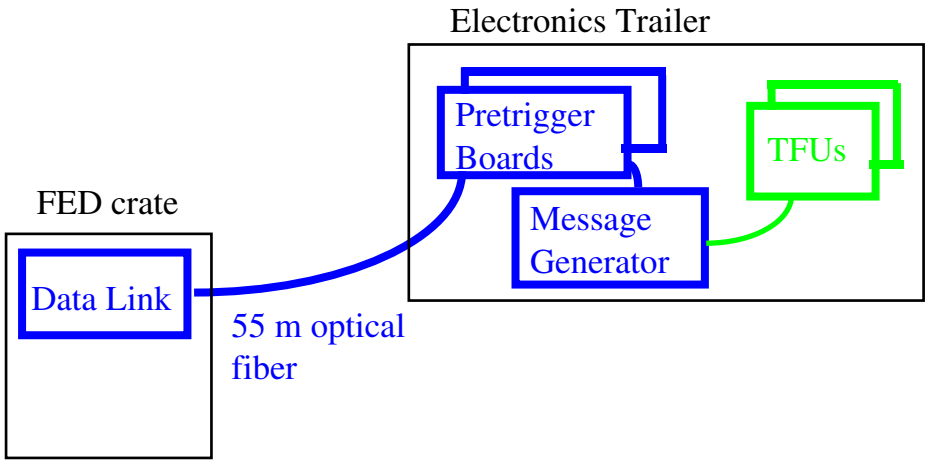
to do:

SHARC Link and CPU control.

Joachim Gläß, Informatik V, Univ. Mannheim, email: glaess@ti.uni-mannheim.de

# High PT Pretrigger

## PROTOTYPE-SERIES




## Status:

| board | design | layout | preseries PCB | production |
|---|---|---|---|---|
| test | ✔ | ✔ | 5 delivered | |
| link | ✔ | ✔ | 5 delivered | Jun. @ DESY |
| pretrigger | ✔ | ✔ | 3 delivered | Jul. @ industry |
| PMG emu | ✔ | ✔ | | started |
| PMG | ✔ | ✔ | P.O. issued | P.O. issued |

**➜ Link & pretrigger board prototypes still expected ~ summer 1998** ← not changed (Oct.)

**(PMG emulator in Nov.)**

# MUON Pretrigger

## TEST SERIES -- VERSION 1

**Pretrigger Link Board (PLB):** ~40

- **Design finished & submitted to industry**

➜ **4 assembled boards expected 15 Aug. '98**

**Pretrigger Coincidence Unit (PCU):** ~40

- **Reduced complexity, added ECAL inhibit**
- **Design will be finished 1 Jul. '98**
- **Production order submitted to industry**

➜ **3 assembled boards expected 1 Oct. '98**

**Pretrigger Message Generator (PMG):** ~20

- Development passed on to v. Staa group

➜ **start prototype testing in Aug. '98**

**The combined MUON pretrigger chain:**

➜ **redesign of all boards almost finished**

➜ **test series production by industry**

➜ **2 pretrigger slices (2x(2+2+1)) will have been built and 1 will be @ DESY by Nov. '98**

# ECAL Pretrigger

**ECAL Pre-Trigger Board:** **~ 128**

- **2 boards of last design iteration under test in Bologna**

- **If okay**

➜ **20 boards at DESY by 1 Aug. 1998**

- **If this pre-series okay**

➜ **20-30 boards/month (Sept. '98 - Jan. '99)**

➜ **whole inner ECAL equipped by 1 Oct. 1998**

# Data Link

**MUON & OTR Link Boards:** ~ 200

**TEST SERIES -- VERSION 1**

- Modified prototype tested with TFU

➜ build test series of 7+33 boards

➜ implementing changes into layout

➜ P.O. has passed DESY purchasing & we are soliciting offers from companies

➜ Plan to have 7 FLT_LBs by 1 Sept. '98

➜ Plan to have 40 FLT_LBs by 1 Nov. '98

**MUON Pixel Mapping Board:**
(for pretrigger & TFU tracking)

- Preliminary board layout exists

➜ submission expected mid July '98

➜ prototype testing until mid September '98

**ITR Link Boards:** ~24

- Prototype test with TFU in June '98

➜ 2 ITR_ FLT_LBs @ DESY in July '98

# FLTSIM

C++ clock level FLT simulation

## Goals:

- **Simulation**
  - ➜ test of algorithms
  - ➜ timing/latency
  - ➜ critical system behavior

  - ➜ efficiency studies for physics runs
  - ➜ test of new triggers

- **Hardware Tests**
  - ➜ troubleshooting hardware on board level for automated tests (w/r/c hardware to software)

- **Commissioning Tool**
  - ➜ Diagnostic instrument
  - ➜ Tune parameters for system optimization
  - ➜ Software hardware comparison on board and system level

# FLTSIM
## Status

| | | |
|---|---|---|
| Preparation | tool selection | ✔ |
| | basic design | ✔ |
| | base class lib | ✔ |
| Pretrigger | MUON | ✔ **(except PMG)** |
| | ECAL | ✔ |
| | HIpT | (✔) **except PMG & geometry** |
| FLT processor | Message mod. | ✔ |
| | TFU | ✔ |
| | TPU | (✔) final debugging |
| | TDU | C code exists |
| Overall system & interfaces | mod. interface | ECAL - FLT ✔ |
| | UI | open |
| | overall system | open |

**Tasks achieved**

**MUON pretrigger**

- **system tests**
- **PCU LUTs for tube chambers**

**Track Finding Unit (TFU)**

- **hardware ↔ software comparison**

(leading to automated TFU board software for mass produced TFUs)

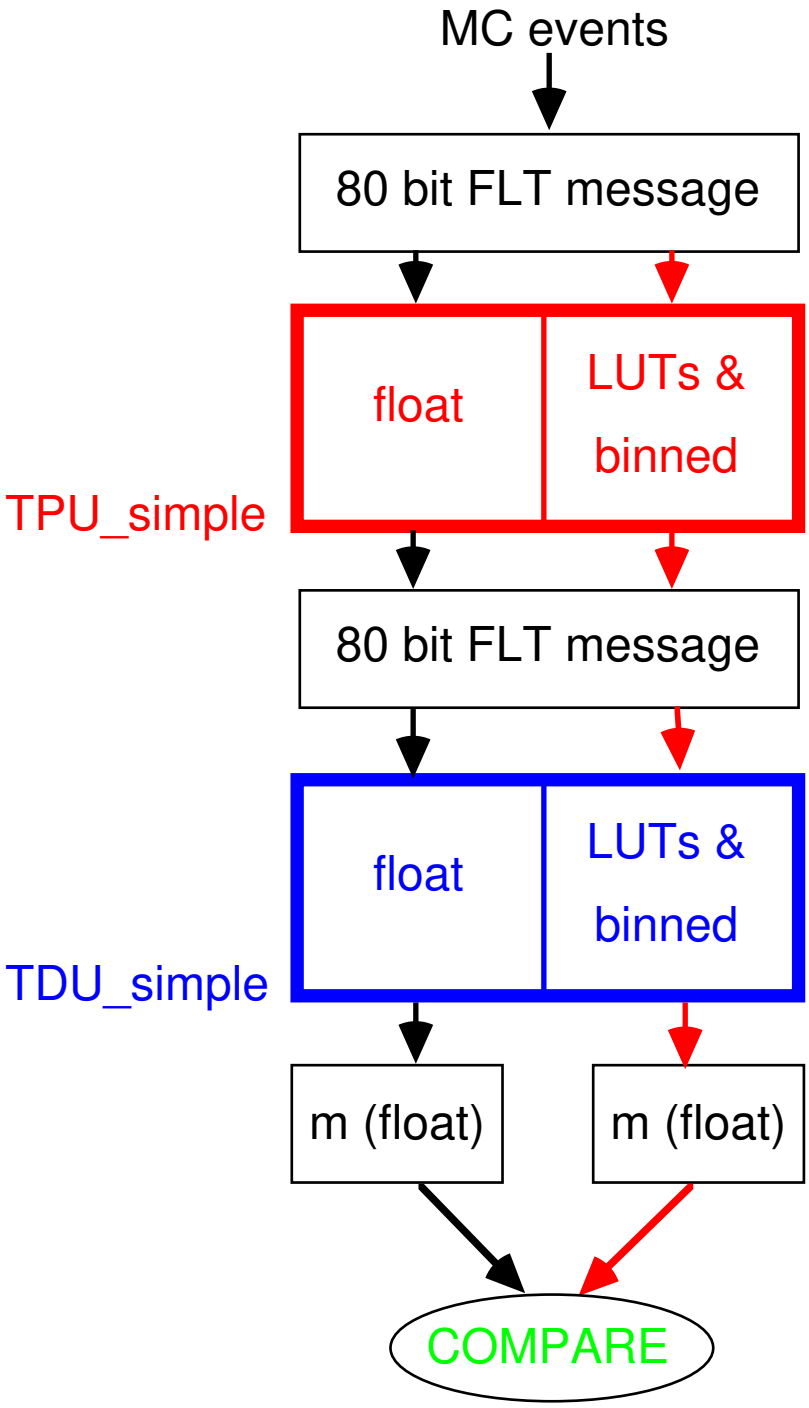
**Track Parameter Unit (TPU)**

- **tests of algorithms**

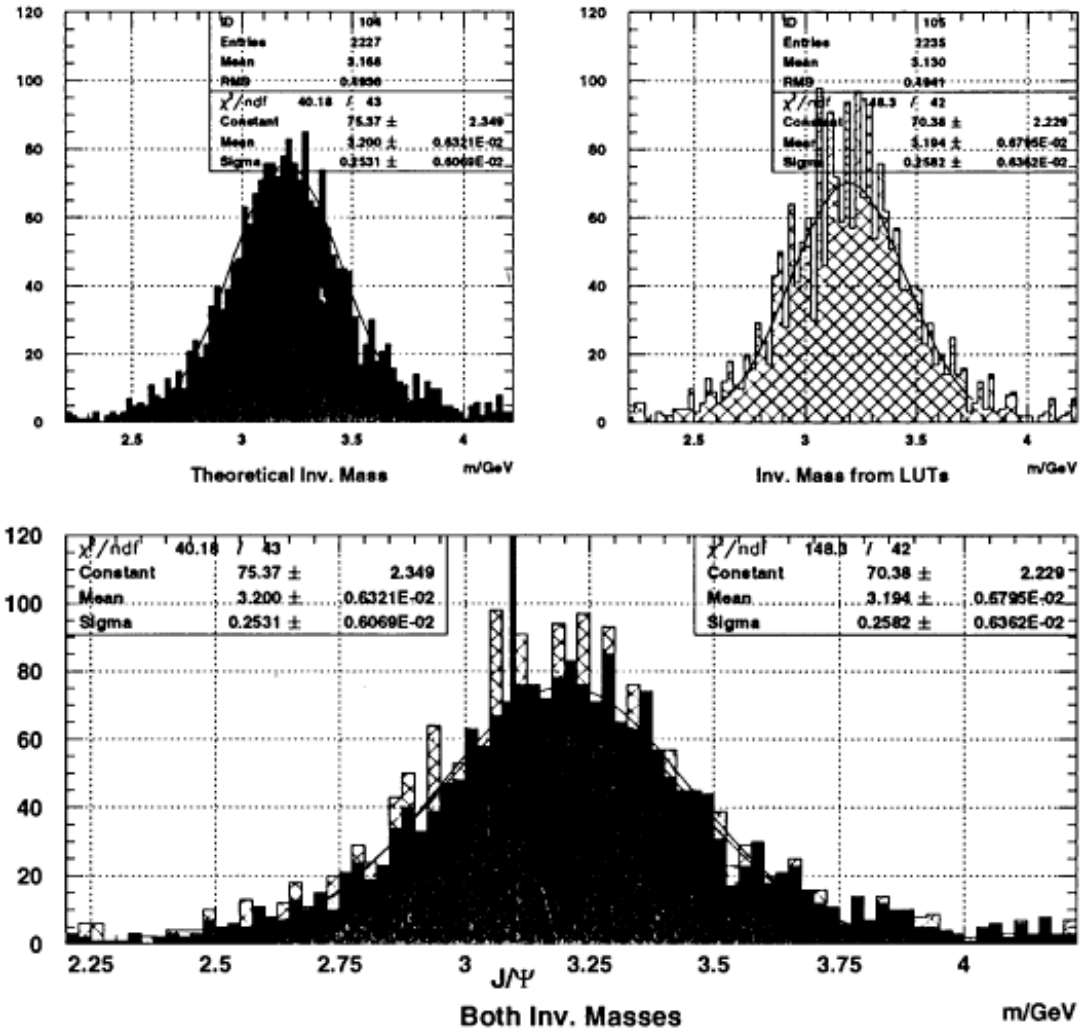
# FLTSIM

- **MC events ($\sigma_M$ = 70 MeV) , parametrized B**
- **hit coordinates @ TC2 & PC1**

➜ **translate into TFU message** (digitization)



## Inv. Mass of J/Ψ → μ+μ− Pairs computed in TDU




Heiko Itterbeck, HERA-B DESY-HH 11/06/98 17.31.10

# Goal for 1998:

# Running FLT System

**Test Components:**

- **ECAL pretrigger** (several slices)
- **MUON pretrigger** (one slice)
- **HIpT pretrigger** (maybe one slice) ← **nice surprise**

- **TFU** (up to 10)
- **TPU** (1)
- **TDU** (1) ← **very likely a reduced capability TDU**

- **OTR data link** (up to 40 FLT_LBs incl. Muon links)
- **MUON data link** (at least for tube chamber)
- **ITR data link** ← **some restrictions due to Helix 2.1**

- **associated detectors**

**Tests:**

➙ **communication of components**
➙ **board and system configuration**
➙ **behavior in real environment** (electronic noise)

➙ **hardware/software (FLTSIM) comparison** (MC and real data)
➙ **tracking** ← **hmmmmm....**

➙ critical system behavior
- message congestion
- inefficiencies
- high rate

# Commissioning ’98

•• First Steps ••

## At laboratory of designers:

- **test boards in lab**
- **develop stand alone tests**
  - **➜ test bench for hardware integrity (for local, in-lab tests)**
  - **➜ automated stand alone test (using software that runs at the experiment)**
- **test interconnection to other system(s) in lab environment**

## At DESY:

- **run automated stand alone test**

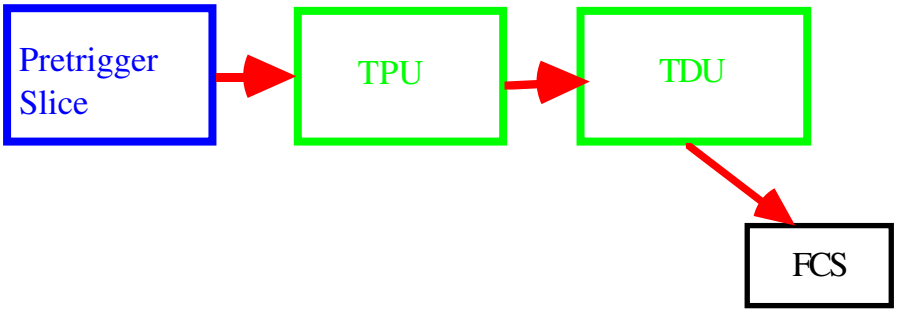
(push button ➜ wait ➜ board pass/fail ➜ get new one or use board)

- **verify interfaces to other test components**
  - **➜ message links** (FLT_TB)
  - **➜ data links** (also FLT_TB ?)
- **phase A - F**

# FLT in '98

## Commissioning ≠ Physics

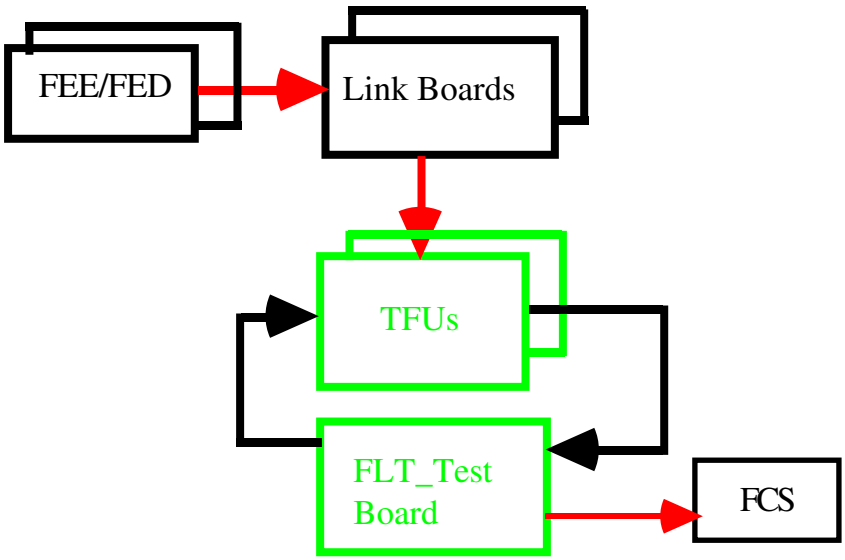
## (A) Message Links:



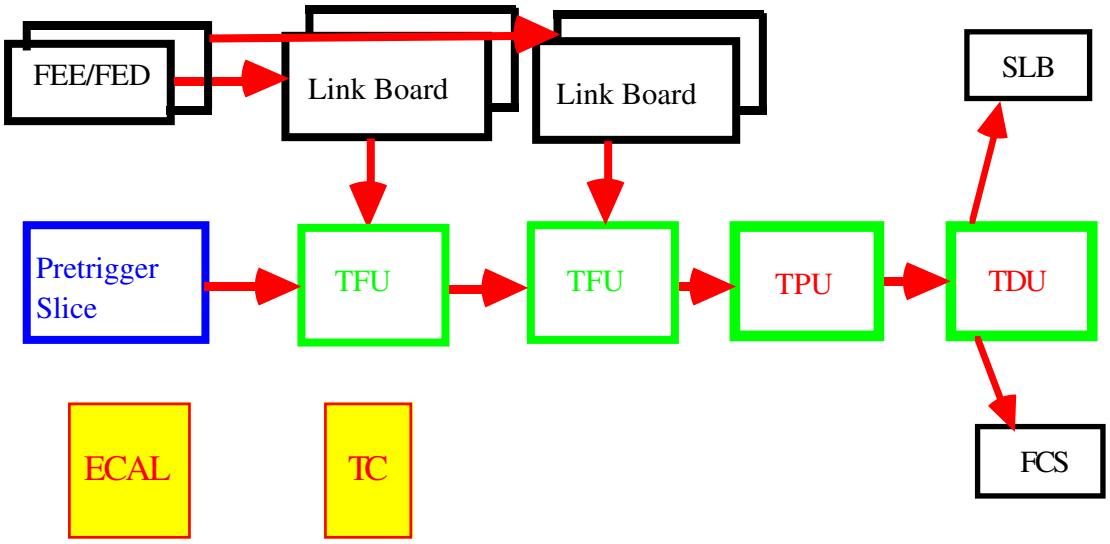

➜ "physics"

**fall back solution → use Test Board as TDU**

## (B) Data Links:



# (E) Track Finding:




**Commissioning ⇒ Physics**

# Summary

**The HERA-B First Level Trigger is still well on its way!**

**TFU and TPU are out of the critical path. TDU still late, but progress has been made.**

**Disasters due to lack of manpower could so far be avoided by redistributing the tasks within and inbetween FLT groups.**

**Our focus is shifting from hardware to software.**

**Having a reliable system in 1999 requires a test of the entire FLT chain.**