SLT status

M. Medinnis

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Since Rome...

- Algorithm development
  - New event sample
  - Further development of FLT-refit code
  - Further development of silicon code
- Requirements document update
- Global design work for SLT/DAQ/farm system
  - A proposal for a message handler
  - A proposal (JGZ) for SHARC system software
- SHARC board, almost...
- SHARC $\leftrightarrow$ C104 interfaces

New event sample

signal: $B^o \rightarrow J/\psi K^o_s, J/\psi \rightarrow e^+e^-$

- B^o+ 4 minimum bias
- 220 events produced
- 101 after FLT

background:

- 5 minimum bias interactions / event
- 45,000 interactions $\Rightarrow$ 9,082 events
- 128 events after FLT (low mass: $M > 1.75$ GeV
- 33 events after FLT (high mass: $M > 2.75$ GeV

Digitization resolution:

- Outer tracker: 200μm
- Inner tracker: 60$\mu m \cdot \sqrt{N_{strips}}$

¡**FLT RoI data (from L1simu):**

- momentum
- position and size of RoI

Old (not Arte) framework

FLT Refit algorithm

Kalman-filter inspired:

- Start with RoI's given by first level trigger
- Follow track through chambers behind magnet (PC1-PC4, TC1, TC2) (all planes)
- Check all hits in original (FLT) RoI
- Evaluate a χ^2 for each hit added
- Evaluate $Q = N_{holes} + 0.05 \cdot \chi^2$
- Require:
  - Total number of missing hits ("N_{holes}") ≤ 5
  - Number of adjacent holes ≤ 2
- Propagate only N best candidates (based on Q)

For results reported in Rome, only the x-view chambers were used.

Since Rome, stereo planes added:

1. Perform x-view filter as before
2. Fix x-view parameters
3. Propagate track through stereo planes

Silicon tracking algorithm

Ancestry:

Code originally written for estimates given in TDR (FORTRAN)

Translated to C and improved, benchmarked on various RISC & DSP platforms

New, since Rome:

Transformed into L2simu framework and further improved

Track following/updating procedure essentially unchanged from the TDR

Filtering (track rejection criteria) extensively changed

New results on dependence of efficiency & required processing time on:

Track rejection criteria

Silicon hit efficiency

Alignment errors

Processor/Architecture Decision

- Theoretically decision due this spring
- Can't happen:
  - No SHARC board
  - No concrete proposals for other hardware
  - Not enough benchmarks: need hardware, need additional code
  - Support software lacking (only proposals exist)

Is this disastrous?

Propose:

Decide by summer on configuration for '97 run.

Continue to develop other ideas.

Decide on final configuration after '97 experience

for 1997:

processor: SHARC (or RISC?)

SLB $\leftrightarrow$ SLT link: SHARC links or C104

algorithm: developed version of HT's Kalman filter (FLT-refit)

configuration: needs thought, work, benchmarks

support software: lots of work needed here (but also needed by DAQ for '96 run)

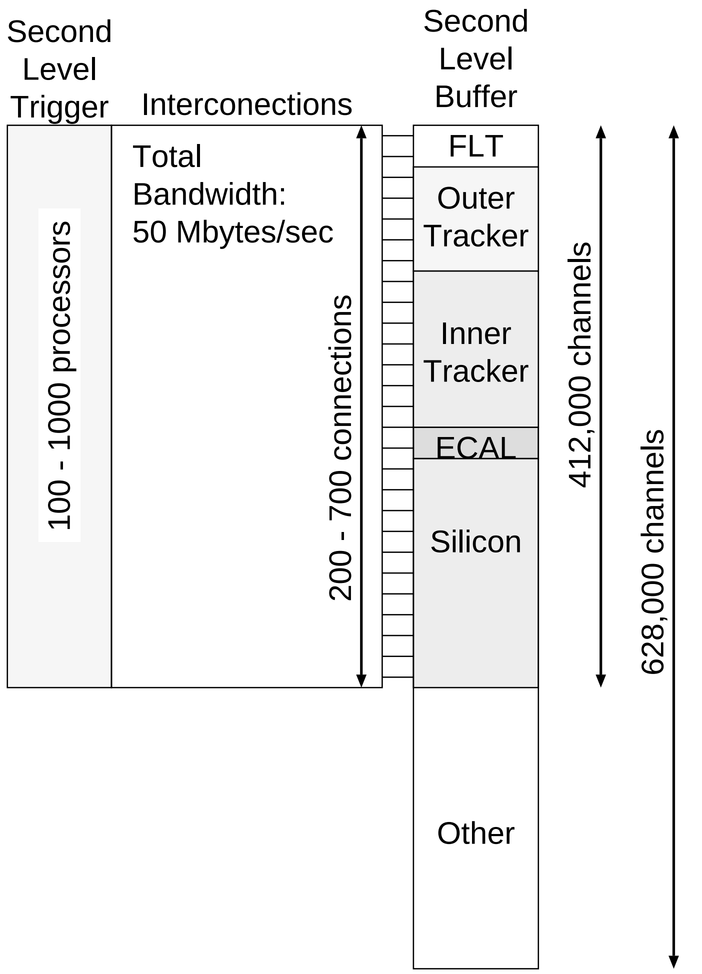
for 1998 and beyond:

processor/configuration: if it isn't the SHARC, what? need concrete proposals, support software, benchmarks

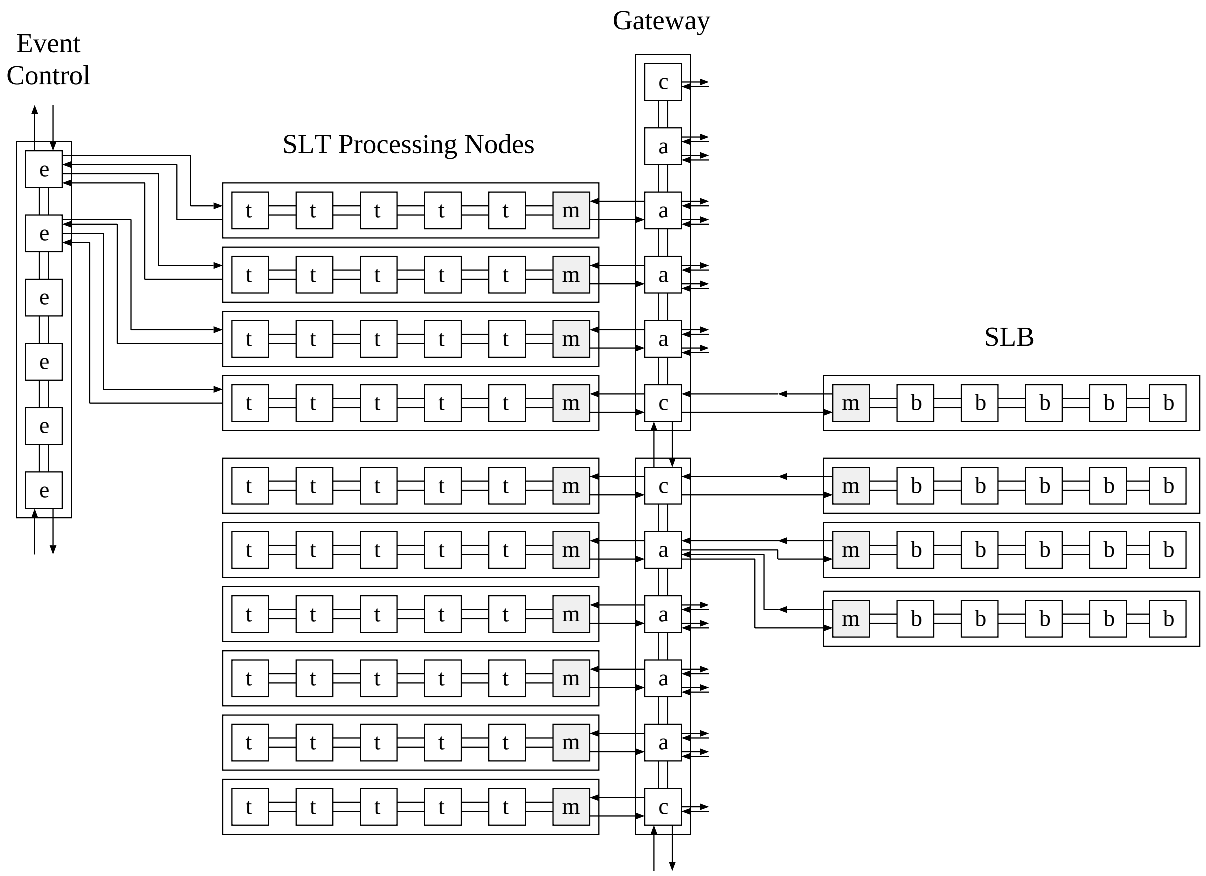
algorithm: HT + JDH/SE + ... or ?

...I don't think so.

Interconnect network



A SHARC link solution



(Not the only way to build a switch with SHARC boards.)

A backup solution (C104 switch)

C104:

- A 32 channel switch
- Each channel is bidirectional
- 10 Mbytes/sec per channel
- based on DS Links

Advantage over the SHARC

- Better connectivity (more channels connected per chip)
- Potentially lower latency
- Lower overhead (for large switches, no CPU intervention inside switch)

Disadvantage

- Introduces a new element into the system
- Lower bandwidth per link (10 Mbytes vs. 40 Mbytes)

Two groups (Zeuthen & Copenhagen) are working independently on SHARC $\leftrightarrow$ DS Link conversion boards.

Conclusions

- FLT refit gives $> 5x$ rejection for efficiency $\approx$ 90%
- SHARC board almost there
- Next: map algorithm (FLT refit with high priority) to target platforms
- Understand latency: benchmarking
- produce SHARC-specific software needed (in collaboration with DAQ)
- Develop backup solution for SLT/SLB interconnect based on the C104.
- Decide on configuration for '97 this summer
- Postpone final architecture decision until mid '97